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FINAL STUDY REPORT

NAVAL REMOTE OCEAN SENSING SYTEM

(NROSS)

STUDY

PERFORMED FOR

JET PROPULSION LABORATORY

PASADENA CALIFORNIA

UNDER SUBCONTRACT NO. 956524
And
NASA CONTRACT NO. NAS-7-100

By

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SYSTEM (NROSS) STUDY Final Report (General
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GENERAL  ELECTRIC

TECHNICAL SUPPORT DEPARTMENT
SPACE SYSTEMS OPERATION
P.O. BOX 8555
PHILADELPHIA, PA 19101

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SECTION 1
INTRODUCTION

SECTION 1

INTRODUCTION

The following report represents the results of the Scatterometer study task under Jet Propulsion Laboratory (JPL) contract number 956524. The objectives of the study were (1) to define a set of hardware similar to the Seasat A configuration and requirement and suitable for installation and operation aboard a NOAA-D bus, and (2) to provide a budgetary cost for one (1) protoflight model.

The scatterometer sensor is currently conceived as one of several sensors for the Navy Remote Ocean Sensing System (NROSS) Satellite Program.

Deliverables requested as part of this study effort were to include a final report with appropriate sketches and block diagrams showing the scatterometer design/configuration and a budgetary cost for all labor and materials to design, fabricate, test and integrate this hardware into a NOAA-D satellite bus.

The initial schedule called for completing the study and delivery of the final report by May 31, 1983. However, problems encountered in the development of the budgetary cost delayed completion of the study by approximately ten (10) days to June 8, 1983.

The "budgetary cost" requested by JPL and submitted with this report are to be considered as Not-To-Exceed (NTE) costs.

The hardware configuration selected during this study is similar to that developed during a study performed for NASA-Goddard Space Flight Center (GSFC), and completed, to a lesser extent, in March of 1982. This configuration consists of two (2) hardware assemblies -- a transmitter/receiver (T/R) assembly and an integrated electronics assembly (IEA). The T/R assembly as currently conceived is best located at the extreme opposite end of the satellite away from the solar array assembly and oriented in position to enable one surface of the assembly to have unobstructed exposure to space. The IEA is planned to be located at the bottom (earth viewing) side of the satellite and will require a radiating plate whose exact dimension will be determined during a preliminary design phase.

Seasat A design concepts are adaptable and will be used in a possible modified form factor for the T/R assembly. The IEA, however, uses a flexible digital technique (versus analog for Seasat) for processing the scatterometer data and is considered a completely new design. The antennas will be similar to SASS scaled to the new frequency and containing one polarization only.

There are available in storage at the General Electric Company some SASS residual hardware in addition to antenna materials, assembly fixtures, shipping containers, and mass models. This material is planned for use during the design/development phase of the NROSS scatterometer. Details to the extent this material can be used for the NROSS program is given in this report.

SECTION 2
SYSTEM ANALYSES

SECTION 2 SYSTEM ANALYSES

2.1 LINK CALCULATIONS

Link calculations are performed based on the σ^0 values updated for the NROSS Scatterometer Performance Specification. The updated instrument design parameters are employed to generate the Doppler cell link parameters, the antenna gain parameter $(G/G_0)^2$, the received power P_R , K_p - value, and the SNR.

where:

σ^0	=	Normalized Radar Cross Section.
G/G_0	=	Ratio of antenna gain at a specific beam angle relative to the gain at the antenna beam center.
P_R	=	Power received at the Scatterometer antenna.
K_p	=	Normalized Standard Deviation.
SNR	=	Signal-to-Noise Ratio at the input to the digital signal processor.

The K_p equation must be modified for digital signal processing. The new value of K_p is then adapted to the link calculation. The optimal number of the Fourier components of each doppler cell and the effects of the long gate are the minimum necessary factors to be considered in modifying the derivation of K_p . Other factors, which are found to influence the K_p estimate, will be incorporated in the K_p equation for the digital signal processor.

2.2 ERROR ANALYSIS AND BUDGET

There are three primary factors which affect the accuracy of the σ^0 measurement. They are communication noise, attitude pointing uncertainty, and instrument processing errors.

2.2.1 COMMUNICATION NOISE

The accuracy of the σ^0 measurement relies on the accuracy of the measurement of the received power P_R . P_R is estimated by computing $(P_{SN} - P_N)$ where

P_{SN} is the estimated power of signal plus noise (S+N) and P_N is of noise power only (N). The error budget of the P_R estimation is given by the equation for K_p as shown:

$$K_p = \left[\frac{1}{N_1} \left(1 + \frac{N}{S} \right)^2 + \frac{1}{N_2} \left(\frac{N}{S} \right)^2 \right]^{1/2}$$

where N_1 is the number of independent samples of signal plus noise power and N_2 is the number of independent samples of noise only power. The following will be resolved and accommodated in the K_p equation:

a. Long Gate Effect

The gate-open period $(t_G)_i$ where $i = 1$ to 6, is fixed for each antenna beam for the whole orbit. The integration period $(t_{SN})_i$ for the signal plus noise is set less than $(t_G)_i$ in order to maximize the return signal power for all cases of spacecraft altitude and pointing angles. During the time period $(t_G)_i - (t_{SN})_i$, only communication noise is integrated which degrades the P_R measurement data. The amount of this degradation will be analytically obtained and incorporated in the K_p equation.

The doppler spread is a function of orbit position in addition to antenna beam. The number of samples per cell will be optimized to insure a valid measurement for each doppler cell throughout the orbit.

2.2.2 ATTITUDE POINTING UNCERTAINTY

The antenna squint angle along with the uncertainty of the S/C attitude and altitude cause uncertainty in the doppler cell area, the value of G/G_0 , and the slant range (R_c) from the spacecraft to the center of the doppler cell. The uncertainty in slant range is taken into account by extending the return gate timing. This wider gate reduces the detected SNR by integrating noise only. The effect of the reduced SNR on K_p will be derived. The measurement error introduced into σ^0 by the changes in cell area and G/G_0 will be defined in terms of the uncertainty of the S/C attitude and altitude and the antenna squint angle through the analysis of the doppler resolution link and G/G_0 .

2.2.3 INSTRUMENT RELATED ERRORS

Instrument bias errors such as antenna, transmitter, receiver, quantizing, gain uncertainty, finite arithmetic and the errors associated with the FFT application will be evaluated and error budgets will be determined for the instrument.

2.3 MEASUREMENT REQUIREMENTS

The NROSS Scatterometer is required to measure the wind speeds of 4 m/sec. at earth incidence angles from 20° to 60° . The expected maximum and minimum power (P_R) will be calculated for worst case values to ensure that the receiver dynamic range is large enough to meet the calculated value at each end of the range. The expected doppler spread will be obtained through the resolution cell link analysis.

2.4 CALIBRATION REQUIREMENTS

The calibration requirements on the factors which critically influence the performance of the Scatterometer will be defined. These factors include K_p - values, dynamic range of the processor, the maximum σ^0 bias error, geometric separation between σ^0 measurements and the swath width.

2.5 RETURN SIGNAL SIMULATION

A computer program will be generated to simulate the Scatterometer return signal present at the antenna. This signal will be used to estimate the system performance of the Scatterometer Processor. A white gaussian noise generator will be used to produce narrowband gaussian noise with variable power level corresponding to the expected Scatterometer return signal power.

2.6 CELL REGISTRATION

The area of interest on the ocean surface that is illuminated by the transmitter fan beam signal is 785.4 km on each side of the spacecraft. This swath will be divided into one near nadir cell and 24 wind vector cells, on each side of the spacecraft for 25 km x 25 Km cell resolution. The relationship between the doppler frequency of the return beam and the corresponding position on the ocean surface is a function of the velocity of the satellite, geometry, transmit antenna, and the rotation of the Earth.

The geometry of the situation dictates that only the 24 doppler cells in the wind vector swath vary sufficiently to require correction. The center frequency of the doppler cells can be found to vary sinusoidally as a function of orbit position. Each doppler cell for each antenna is defined by a unique sinusoid. Thus, for one-half of the spacecraft, 3 antennas x 24 doppler cells or 72 different sinusoids are required to define the behavior of the doppler center frequencies. The center frequency is given by:

$$f_o = f_m + \Delta f \sin \left(\frac{2t}{P} + \phi \right)$$

where

- f_o = doppler center frequency
- f_m = nominal doppler center frequency
- Δf = maximum excursion of the sinusoid
- Δf_a = ascending orbit
- Δf_d = descending orbit
- t = TI

$$T = \frac{P}{2^N}$$

- P = Orbital periods in seconds.
- I = Integer value of T_a/T
- T_a = Time from ascending node for each orbit, sec.
- ϕ = Phase angle of $\pm 180^\circ$ for ascending or descending orbit.

Unique values of f_m , Δf_a , and Δf_d exist for each of 24 cells for each antenna f_o must be corrected for each cell as a function of position in orbit.

An optimal value for N will be chosen from the point of the accuracy of the coregistration and the simplicity of the signal processing.

After an algorithm is established, the error factors affecting the cell registration accuracy will be considered. These include the antenna squint angle, the spacecraft attitude and altitude and the constant change of the

antenna azimuth angle with respect to the spacecraft subtrack. The maximum total error effect caused by these factors will be estimated and this result is applied to determine the necessary time between the successive measurements of each antenna.

The Earth rotation also causes the change of the incidence angle of the center of the doppler cell. An equation will be obtained to describe the relation between the change of the incidence angle and Earth rotation.

An antenna azimuth angle of -115 degrees for Beam 5 will be investigated on the basis of cell registration and digital signal processing.

2.7 DIGITAL FILTERING

A Fast Fourier Transform has been selected to perform Digital Filtering for the MASS Scatterometer. This selection was based on a study performed by General Electric Company under contract for Langley Research Center (PO #L518B and 8163B). Analysis will be developed to determine the effect of the FFT on K_p . These effects include finite arithmetic in addition to the sin X/X filter characteristics. Selection of optimum bandsplitting channels, selection of filter bandwidths, and selection of sample rates and aliasing effects will be optimized.

2.7.1 IF CHANNELS

An equation will be obtained which describes the relationship between the expected doppler signal vs. the signal received interval for each antenna beam. The equation defines the expected variations in the return signal (see Figure 2.7-1).

The return signal will be divided into four IF channels (as illustrated in Figure 2.7-1). In this figure, t_i and s_i ($i = 1, 2, 3, 4$), represent the times when the FFT starts and finishes processing the signal contained in each IF channel. t_i and s_i will be fixed for each antenna beam throughout the orbit. IF_i, the bandwidth B_i , t_i and s_i ($i = 1, 2, 3, 4$) of each channel are the parameters which define the FFT signal processing scheme. A requirement for B_i is:

$$B_1 + B_2 + B_3 + B_4 \leq \text{the maximum doppler frequency spread.}$$

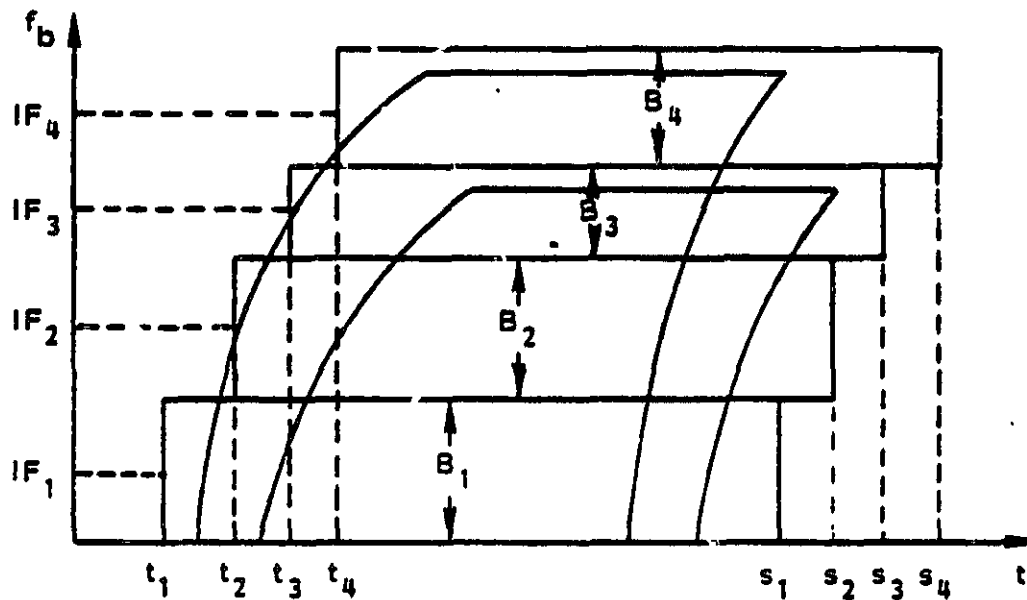


Figure 2.7-1. Doppler Return Vs. Received Time

Since the FFT processor is designed to perform a 256 point FFT on the received signal, the maximum bandwidth (B_i) that can be processed in the i th channel by one FFT is:

$$B_i = 256 \left(\frac{1}{s_i - t_i} \right)$$

If, however, (k) FFT's are being performed during the return signal, B_i is then:

$$B_i = 256 \left(\frac{k}{s_i - t_i} \right)$$

The term $k/(s_i - t_i)$ is the frequency separation of the Fourier components of the FFT. The number of these spectral lines, or bins, accumulated determine the bandwidth of the filter and accordingly, the spatial resolution.

The input and output ports of the FFT will be fixed to 256. Thus the value of B_i fixes the spacing between the Fourier components of FFT, which necessarily determines the number of Fourier components belonging to each doppler cell. The spacing between the Fourier components is such that the σ^0 estimations derived from the P_R measurement by three antenna beams do not degrade the accuracy of the estimation of the wind velocity vector when they are combined.

The IF channel bandwidths to be used for processing the signal of each beam will be determined depending on the maximum expected doppler spread for all conditions.

Another factor which governs the IF channel bandwidth is the frequency components located near the upper or lower boundaries of the IF channels. Due to the differences between the Low Pass Filters (LPF) implemented in each IF channel prior to the FFT Processor, the Fourier components from the different IF channels cannot be combined to obtain a dependable power measurement. A solution will be given by overlapping the IF channels well enough so that any doppler cell will be completely contained in one of the IF channels (see the hatched area of Figure 2.7-2). The overlapping regions will be defined.

2.7.2 TIME-SHARING

A cost effective design of the 256 point FFT Processor dictates a time-sharing technique to process the doppler returned signal for each IF channel. The time period $s_i - t_i$ should be fixed as close to τ_i as possible where τ_i is the time period when the leading edge of the doppler return signal is received by the receiver with the communication noise superimposed on it (see Figure 2.7-3). A baseline time-sharing scheme is shown in Figure 2.7-3. The hatched area in Figure 2.7-3 is either when only the communication noise is processed during S+N measurement period or when the doppler returned signal is ignored although the receiver actually received S+N. The time-sharing scheme will be obtained by minimizing the hatched area.

2.7.3 DOPPLER CELL GENERATION

The return signal will be divided in four distinct frequency bands. Each band will be further subdivided into 256 frequency bins by processing with a 256 point FFT. A total of 1024 frequency bins on power spectral lines will be generated across the total doppler bandwidth. Doppler filters are generated by selecting

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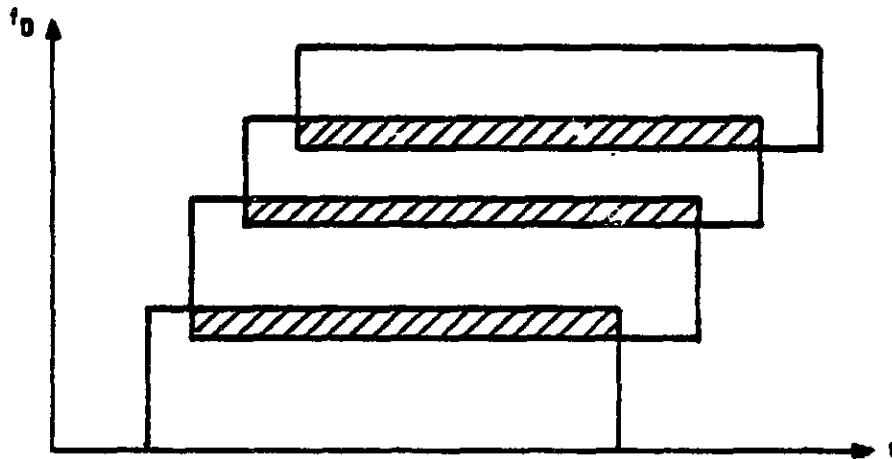


Figure 2.7-2. FFT Overlapping

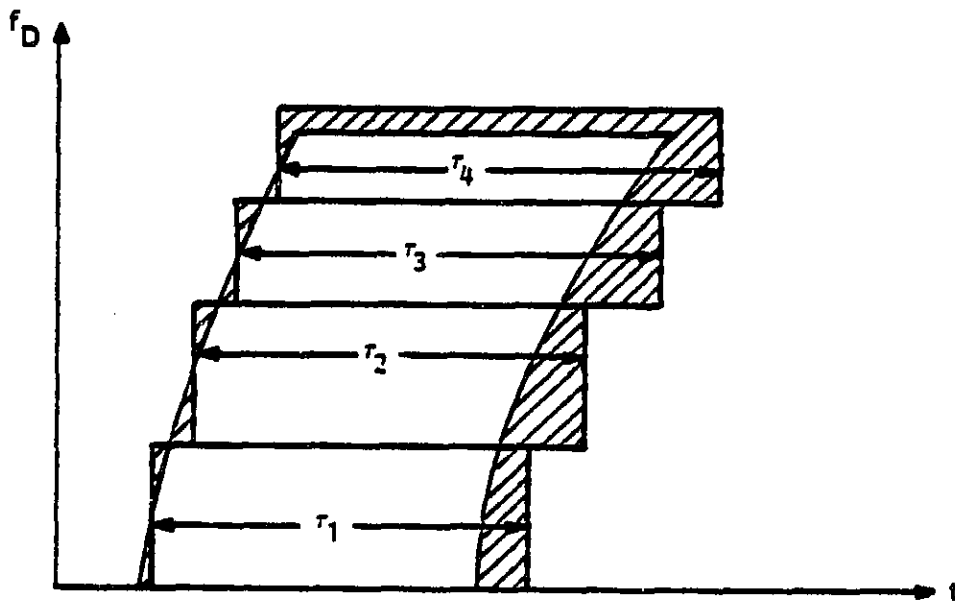


Figure 2.7-3. Baseline Time-Sharing Scheme

the appropriate number of adjacent frequency bins to generate a corresponding doppler cell. This filtering is based on the frequency to spatial relationship required to maintain cell resolution across the ocean surface. The coregistration problem involves adjusting the selection of Fourier bins based on-orbit position. Analysis will be performed to define the effects of interference on adjacent doppler filter cells due to finite bin bandwidth as well as the filter characteristics themselves. Preliminary studies indicate that Hann weighting of the FFT output improves cell to cell isolation significantly.

2.7.4 THE NUMBER OF MEASUREMENT OF S+N AND N

The results of the analyses mentioned so far determine the number of independent samples of the doppler cell and the effect of a long gate for P_{SN} and P_N measurements. The K_p equation will be modified based on these results.

In Appendix B-2 of the NOSS Scatterometer Specification, an attempt was made to obtain an optimal number of S+N and N-only measurements during one measurement period T_M . The updated K_p equation will be applied to improve the optimal number of S+N and N-only measurements, following the same scheme described in Figure 3 of Appendix B-2, NOSS Scatterometer Specification. This method gives the same number of Fourier doppler samples for S+N and N-only measurements while minimizing the K_p values.

2.8 ELECTRONIC CIRCUITS AND GAIN STABILITY

K_p estimation is directly affected by changes of the transmitters power, the transmit wavelength, the antenna pattern, miscellaneous system losses, L_s , and the measured received power P_R . This is known through the equation:

$$\sigma^0 = \frac{64^3 R^4 P_R}{P_{T\lambda}^2 L_s G_0^2 (G/G_0)^2 A}$$

where

- R = The range to the center of the cell.
- A = Cell area.
- G_0 = The peak antenna gain.

The effect of the degradation of P_T and λ on σ^0 equation will be obtained through the σ^0 equation and will be checked by the test results.

The stationarity of the receiver/Scatterometer Processor relies on the stability of the receiver circuit, A/D converter, FFT processor, Hanning window and the other electronic circuits of the Scatterometer Processor. The gain stability of the Receiver/Scatterometer Processor as a whole will be obtained through test.

2.9 IN-ORBIT CALIBRATION REQUIREMENT

The instantaneous performance characteristics of the transmitter, the receiver and the signal processor are the fundamental factors that dominate the accuracy of the σ^0 measurement. The basic concept employed to determine the optimal measurement rates on board is to calibrate as frequently as possible in order to guarantee the instrument performance. However, since calibration runs reduce the amount of valid data, the calibration rate is selected to maximize data acquired while maintaining system performance.

The transmitter output power will be continuously monitored and downlinked in the TLM data stream as it was done for the Seasat A Scatterometer. The Receiver/Scatterometer Processor will be calibrated with a calibrated noise source. The analysis and the verification of the stability of the Receiver/Scatterometer Processor will be used to determine the calibration period in addition to the number of noise samples required to maintain valid noise only data.

SECTION 3
HARDWARE CONFIGURATION

SECTION 3

HARDWARE CONFIGURATION

3.1 MECHANICAL DESCRIPTION

The NROSS Scatterometer consists of a Transmit/Receive Assembly, an Integrated Electronics Assembly (IEA) and six Fan Beam Antennas, with associated waveguide and wire harness interconnections. The total weight of the instrument will be approximately 246 lbs. (112 kg), not including antenna deployment mechanisms and launch restraints.

3.1.1 SATELLITE DESCRIPTION, INTERFACES AND ASSUMPTIONS

For purposes of this study, it is assumed that the Scatterometer will be carried by a NOAA-B type spacecraft. The Integrated Electronics Assembly (IEA), a 20 lb. (9.1 Kg) box dissipating 32 watts, mounts on the earth facing side of the spacecraft and requires 1.6 ft² radiation area.

The T/R assembly which weights 120 lb. (54.4 Kg) and dissipates 112 watts, requires a cold space view and a louvered radiator of 5.3 ft.² area.

The six antennas will be deployed from a point near the T/R assembly, to minimize waveguide length and weight. Figure 3.1-1 shows the locations of the Scatterometer hardware. It is assumed that the Scatterometer components will be provided with independent thermal controls, and will be isolated from the spacecraft structure so that their heat will not be dissipated to the vehicle.

Hard mounting points will be provided on the Spacecraft Equipment Support Module, to attach the 120 lb. T/R assembly and the 20 lb. IEA, by means of thermally insulating standoffs.

3.1.2 SENSOR MECHANICAL CONFIGURATION

3.1.2.1 Transmit/Receive Assembly

The T/R assembly contains the RF components of the Scatterometer, all mounted to a 32 in. x 24 in. plate, which acts as support and thermal integration structure. The equipment arrangement is shown in Figure 3.1-2. The T/R assembly will be configured to mount on the -Z side of the ESM, with waveguide ports located on the +X and -Y faces of the box.

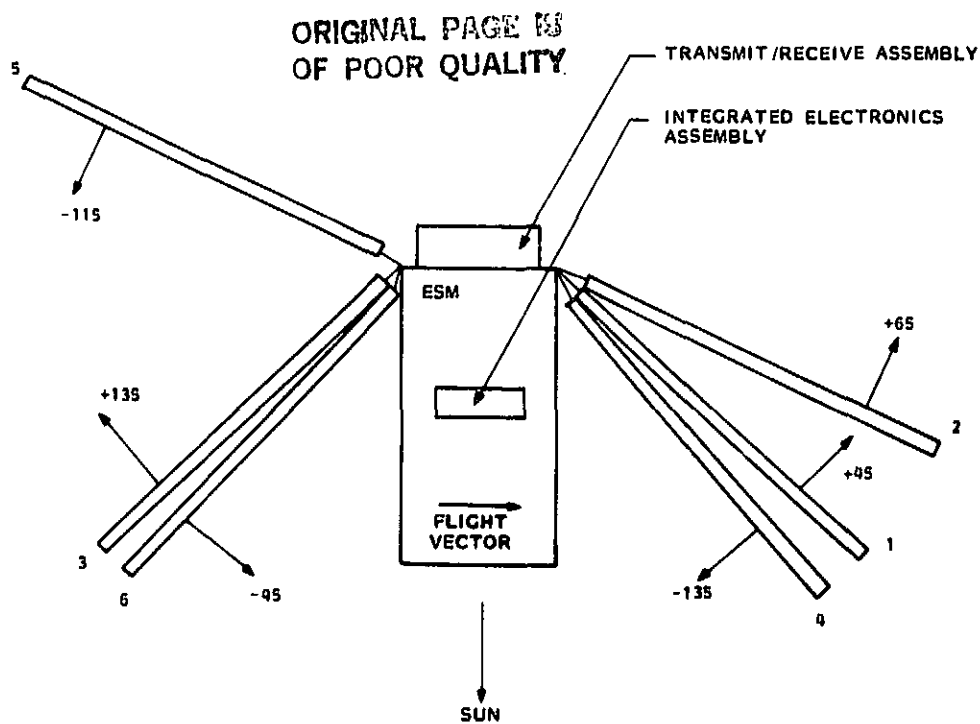


Figure 3.1-1. Scatterometer Arrangement (Looking at the Spacecraft From The Earth)

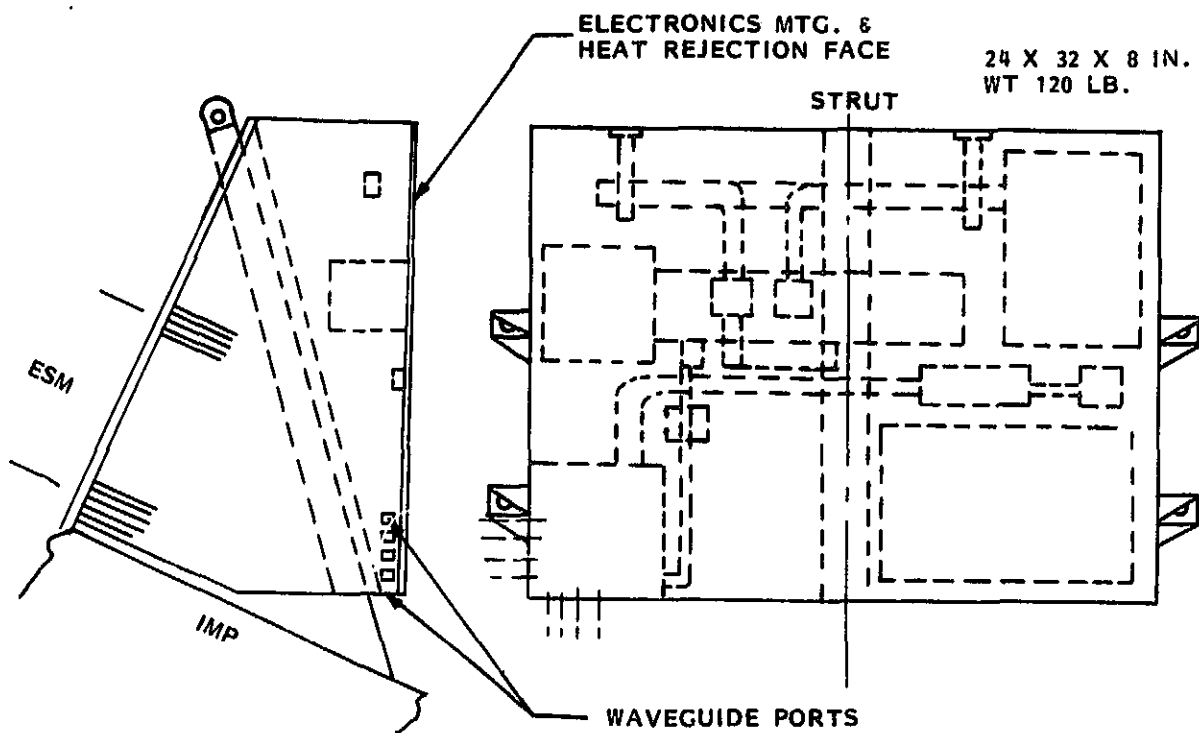


Figure 3.1-2. T/R Assembly Mounting

Table 3.1-1 tabulates the major components of the T/R assembly, with their weights and power dissipations. Interconnecting waveguide, wire harness and structural components are not currently defined, but will be similar to components of the NOSS Scatterometer. The principal difference is the support structure which attaches the T/R assembly to the spacecraft. This will be a new design, developed to meet program thermal and environmental requirements.

Table 3.1-1. T/R Assembly - Components

	WEIGHT (LB.)	THERMAL DISSIPATION (WATTS)
SS/LO	7.50	12.0
FREQUENCY SOURCE	1.69	10.0
HVPS	24.15	30.5
TWT	14.99	37.1
4 PORT CIRC. }	0.31	--
DIODE MIXER }		
INPUT CIRC.	0.14	--
OUTPUT CIRC.	0.25	0.3
DIRECT DETECT.	0.31	0.9
ASM	5.30	6.0
LNA	.88	14.2
ISO ADAPT. 1	0.19	--
DOWNCONVERTER	0.20	--
ISO ADAPT. 2	0.19	--
LOW PASS FILTER	0.18	0.3
W/G COMP. 1	0.30	--
BAND PASS FILTER 1	.308	--
W/G COMP. 2	.308	--
CAL. NOISE SOURCE	.278	0.3
CURRENT SOURCE	.136	--
BAND PASS FILTER 2	.132	--
BAND PASS FILTER 3	.102	--

3.1.2.2 Integrated Electronics Assembly (IEA)

The IEA provides a lightweight, rugged package to contain the low voltage power supplies, digital control circuitry and signal processor of the Scatterometer. It consists of an aluminum dip-brazed housing, having provision for 19 plug-in printed circuit assemblies, 3 hard wired chassis and a modular, bolt-on power supply. Table 3.1-2 shows the number of piece parts, and number of boards/type boards for each principal IEA function.

Table 3.1-2. IEA Digital/Discrete Characteristics

	PARTS	QTY/DESIGNS	MODULES	DRAWINGS
IEA	--	--	--	26
DC/DC Converter	142	1/1 Type D	7	23
Dig. Controller	539	5/5 Type A	--	17
Scatt Processor	1355 (IC)	14/1 Type A	--	33
Total	2036	19/1	7	99

Interconnection is accomplished by a multi-layer "motherboard" backplane, which carries power and internal signals only. Each circuit board which communicates to the external harness is equipped with a flexible cable interface, soldered to a connector hard mounted to the board frame. This concept originated in the SASS IEA and was refined and used on several Electronic Packages on the DSCS III vehicle. Figure 3.1-3 shows the general arrangement and number of circuit boards per subassembly. It has proven to be a reliable, producible packaging arrangement, easy to disassemble for troubleshooting or replacement.

The basic modular unit of the IEA is a multi-layer printed circuit board, meeting MIL-P-5510 requirements, which is capable of mounting 60 logic IC's, or an equivalent arrangement of discrete parts, IC's and hybrids. Parts are mounted by planar solder reflow to enhance producibility and maintainability. Attachment and mounting methods meet or exceed the requirements of NHB5300.4 (3A-1).

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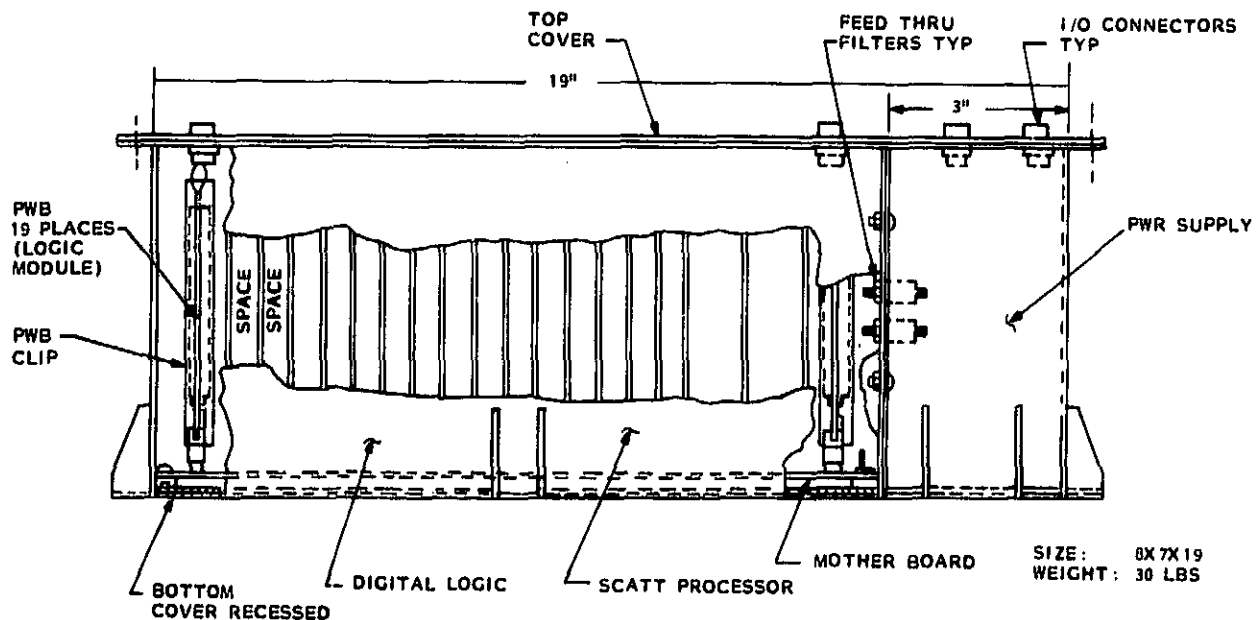


Figure 3.1-3. Integrated Electronics Assembly

The IEA thermal dissipation is estimated to be 97 watts which must be radiated to space. This will cause major revisions in the design of the IEA structure from the NOSS baseline. A detailed thermal model will be generated for the IEA to guide the packaging design, in order to assure that all parts will operate within their derated temperature limits.

The design of the IEA structure will assure that the parts and circuits enclosed will not be subjected to excessive deflections or "g" levels. A stiff, light-weight dip-brazed aluminum housing is proposed, with viscoelastic dampers applied as needed to limit structural responses to input vibration and shock. A detailed stress and dynamics analysis is planned to verify the packaging design. All materials will be reviewed and approved for program use. Outgassing characteristics of organics will not exceed 1.00% total weight loss or 0.10% VCM.

The IEA will be designed so as to minimize the use of magnetic materials and will be vented to assure safe pump-down during the ascent environment.

Hybrid Microcircuits

Hybrids used in the IEA will be similar to those used in the Galileo NMS Program, which were designed and manufactured by GE-SSD.

Design Control

Design control for packaging is provided by the use of GE-SSD S30,000 series specifications. All printed circuit and black box assembly and harnessing criteria are specified in these documents, which are referenced on drawings. Maintenance of these standards is coordinated across programs by the GE-SSD Standard Board, consisting of senior representatives of Engineering, Manufacturing and Product Assurance functions.

3.1.3 THERMAL

The following is a tabulation of the thermal specification for the NROSS Scatterometer requirements.

The Transmit/Receive Assembly shall be mounted on the -Z end of the spacecraft. The surface normal of the radiating surface of the box will be elevated 23° above the -Z axis toward the -X axis.

A sun shield will be located around the four sides of radiating surface of the Transmit/Receive Assembly. The sun shield for the IMP radiator will constitute one surface of the Transmit/Receive Assembly sun shield. This surface, as well as the other three surfaces of the Transmit/Receive Assembly sun shield, will be covered with multilayer insulation.

The mounting surface of Transmit/Receive assembly which constitutes the primary radiating surface for the box assembly, will be one quarter inch thick aluminum.

The mounting surface of the Transmit/Receive assembly box will have dimensions of at least 32" by 24".

The radiating surface of the Transmit/Receive assembly box will be covered with one or more bi-metallic actuated louver assemblies. The effective emissivity of the louver assembly, based on the total louver assembly footprint, will be at least $\epsilon = 0.6$ when fully open.

Except for the louver surface of the Transmit/Receive assembly, the other five surfaces of the box will be covered with a multilayer insulation blanket with an effective emissivity no greater than $\epsilon = 0.025$.

The Transmit/Receive assembly will be conductivity isolated from its support structure by means of thermal bushings. The quantity and dimensions of the bushings is TBD.

The LNA oven will be conductivity isolated from its mounting surface in order to limit conduction to the panel and, therefore, heater power requirements. This isolation shall also include two sections of stainless steel wave guide to limit conduction via this path.

The LNA will have a thermostatically-controlled heater attached to maintain its temperature at a nominally constant level. The thermostat on-off dead band will not exceed 3°C . A tentative set point of 32°C to 35°C is selected. This circuit will consist of a control and over-temp. thermostat circuit in series with the heater. Should reliability indicate, this circuit may have to be redundant.

The crystal of the frequency standard will be maintained at a constant and precise temperature by means of an internally designed heater/ thermostat. The tentative set point for this thermostat is 65°C .

The wave guides entering and leaving the Transmit/Receive assembly will be wrapped with multilayer insulation from the box interface to the antenna interface. Any cable runs between the Transmit/Receive assembly and the IEA assembly will be similarly wrapped with multilayer insulation.

Subject to more detailed analyses, a protective heater circuit or circuits shall be mounted to the Transmit/Receive assembly mounting plate to limit its minimum temperature to -25°C in the off mode. This circuit will be thermostatically-controlled (control and over-temp. thermostat). A tentative heater size of 25 watts is specified.

The IEA assembly will be mounted to the +X surface of the NOAA-D.

The primary mounting surface of the IEA will be earth-facing and will serve as a space radiator.

The IEA assembly will be thermally isolated from its mounting structure by means of thermal bushings.

Except for the earth-facing radiator, the IEA box will be covered on the remaining five sides, with a multilayer insulating blanket with an effective emissivity less than 0.025.

The radiating surface area of the IEA box will be at least 1.6 Ft^2 .

The IEA radiator will be covered with 5 mil silvered teflon or optical solar reflectors (OSR).

All components in the Transmit/Receive assembly box and the IEA box with significant power dissipation will be mounted with thermally conductive interface material between the box and its mounting surface.

The IEA box will be fitted with a thermostatically-controlled heater to maintain its temperature above -25°C during powered-down conditions. This circuit will contain a control and an over-temp. thermostat wired in series with the heater. Should reliability analysis indicate a need, this circuit may have to be redundant.

3.1.4 MECHANICAL GSE

The Mechanical Ground Support Equipment (MGSE) required for the NROSS Scatterometer Electronics is listed in Figure 3.1.4-1. This equipment will be similar in function and design to the SASS Scatterometer MGSE supplied by GE for the Seasat Program. In addition to listing the MGSE items, Figure 3.1.4-1 also tabulates the quantity required, heritage from the SASS Program, and applicable remarks. The following paragraphs provide a function and conceptual description of each item. MGSE required for the antennas is described in Section 3.2.2.

3.1.4.1 Shipping Container

The Shipping Container will provide protection and a handling capability for the Electronics Boxes during all phases of transportation and storage. The design will be similar to the SASS shipping container defined on GE Drawing 47D235021-SC-1. The construction is of exterior plywood with a hinged cover and a weather gasket at the junction between the cover and lower portion, to preclude the entry of contaminants into the box when closed and latched. Metal corners, handles, latches, and hinges comprise the hardware items for the container and the bottom of the box contains skids for fork lifting.

Provisions for shock mounting the Electronics Boxes are also provided. The Electronics Boxes are mounted to the handling frame which serves as a shipping fixture. The handling frame is attached to the shock mounts. The handling frame also contains provisions for mounting a 15G recording accelerometer.

The handling frame and the Electronics Boxes will be wrapped and sealed in a polyethylene bag containing activated desiccant packages, to maintain a low humidity environment during shipment or storage. This wrapping shall be

ITEM	QTY.	SASS HERITAGE	REMARKS
M1 SHIPPING CONTAINER	1	470235021-SC-1	THE ELECTRONICS BOXES WILL BE MOUNTED ON A HANDLING FRAME, ITEM 2A, WHEN IN SHIPPING CONTAINER.
M2 HANDLING DOLLY	1	47J235000-DY-01	DOLLY CONSISTS OF LOWER FRAME AND RE-MOVEABLE HANDLING FRAME, ITEM 2A.
M2A HANDLING FRAME	1	47J235000-DY-01	ONE ADDITIONAL HANDLING FRAME WILL BE REQUIRED TO SUPPORT THE ELECTRONICS BOX IN ITS SHIPPING CONTAINER.
M3 HANDLING SLING	1	47E235010-SL-01	
M4 MASTER DRILL JIG	2	TDL-1406	MASTER DRILL JIGS WILL REMAIN IN THE CUSTODY OF GE AND WILL ONLY BE USED TO VERIFY ITEMS 4A.
M4A DRILL JIG	4	TDL-1406	THESE DRILL JIGS WILL BE THE ITEMS USED TO DRILL HOLES INTO THE ELECTRONICS BOXES AND IN THE S/C STRUCTURE.

Figure 3.1.4-1. Scatterometer Electronics Box Mechanical GSE

considered a consumable item, subject to replacement when it is no longer serviceable. The wooden material of the container will be treated, primed and painted to provide required preservation.

A nameplate per GE Drawing NP206401 will contain the following information:

"Shipping Container - T/R Assy and IEA"

Model "NROSS Scatterometer"

DWG. - (As Applicable)

NROSS Contract No. (as applicable)

This nameplate will be permanently attached to the lid of the shipping container.

Additional information such as handling, lifting and tie down instructions, along with the weight of the loaded container, shall be stenciled on the exterior of the box at appropriate locations.

This container will be considered a reuseable item, and with reasonable care, should have a service life of five years.

3.1.4.2 Handling Dolly

This dolly will provide support and limited mobility to the T/R assembly during assembly and testing. It shall consist of a lower framework with trunnion posts and removeable handling frame, and shall be similar in concept to the SASS Instrument Dolly, defined by GE Drawing 47J235000-DY-01. The low framework shall contain lockable, brakeable casters at each corner to provide maximum maneuverability, and the trunnion posts shall contain retractable locking pins to permit the handling frame to be locked in either a horizontal or vertical attitude.

The removable handling frame will contain the Electronics Box Interfaces and will be double as a shipping fixture as described above. The dolly will be constructed of weldable structural aluminum to preclude the need for painting, and all hardware shall be stainless steel.

3.1.4.3 Handling Sling

This sling will provide the capability to lift the Electronics Box during the various phases of final assembly and systems testing. It will resemble, in concept, the SASS Sling defined on GE Drawing 47E235010-56-01. It will consist of a single spreader suspended by a double cabled pear link, with two cabled risers at each end of the spreader. The interface between the sling and the T/R assembly will utilize attach fittings which can be secured to lift points on the box. The sling will be proof loaded to 2-1/2 times the maximum load it will be expected to lift, and will be permanently marked with appropriate proof load and safe load information. The sling shall be constructed of non-corroding materials to preclude the need for painting.

3.1.4.4 Master Drill Jigs

These jigs will provide the agreed upon interface between the NROSS Scatterometer Electronics Boxes and the NROSS spacecraft structure.

- a. Two Master Drill Jigs which will be used to check and validate the other four drill jigs.
- b. Four drill jigs: two to be used by GE for installing the interface holes into the T/R assembly and the IEA, and two to be used by the NROSS spacecraft contractor for installing the interface holes in the spacecraft structure.
- c. All of the drill jigs shall be of precision aluminum plate with interface hold locations bushed as required.
- d. Identification markings and usage instructions shall be permanently etched or engraved at appropriate locations on the drill jigs.
- e. Each drill jig shall have its own storage/shipping container to protect it from unfriendly environments, mishandling or damage during periods of non-use or during transport.

3.1.5 STRUCTURAL/THERMAL

Detail structural and thermal designs and analyses for the Electronics Package, antennas and interconnection waveguide and harness assemblies, will be conducted for the Protoflight Model (PM). The PM Electronics Package will also be used to develop internal waveguide and harness layout, eliminating the need for a separate mockup.

Structural and thermal activities for the protoflight of the Electronics Assemblies include production liaison during fabrication and assembly, and support and monitoring of the qualification and acceptance tests to be performed on the hardware.

Fabrication and testing of the antennas will be conducted at the antenna contractor's facilities.

3.1.5.1 Structural

Design and analysis of the Electronics Packages and antenna structures will be performed by the instrument contractor. It is assumed that interconnecting waveguides and harness designs will be developed by the vehicle contractor, based on information provided by the instrument vendor (GE).

The SCATT instrument will meet all performance specifications during the required three in orbit life after the exposure to the pre-launch, launch, and orbital environments.

The pre-launch environments include: fabrication, integration, qualification and/or acceptance tests, handling, storage, transportation, and launch site tests.

3.1.5.1.1 Random Vibration

The expected vibration exposure at launch is enveloped by the power spectral density tabulated in Table 3.1.5-1.

Table 3.1.5-1. Random Vibration Flight Levels

All Instrument Axes at Mounting Interface	
<u>FREQ. (Hz)</u>	<u>PSD (g²/Hz)</u>
10 - 20	0.0
20 - 80	Increasing at 10 dB/octave
80 - 600	0.04
600 - 2000	Decreasing at 10 dB/octave
Composite	7.0 grms

3.1.5.1.2 Quasi-Static Loads

The SCATT instrument will be designed to withstand the quasi-static loads specified in Table 3.1.5-2. The listed factors of safety will be applied.

Table 3.1.5-2. Quasi-Static Loads (g)

<u>Event</u>	<u>Direction*</u>			<u>Comment</u>
	<u>X</u>	<u>Y</u>	<u>Z</u>	
Lift-Off	± 6.5	± 3.0	± 5.0	Any Combination
<u>Factors of Safety</u>				
Yield	1.4			
Ultimate	1.8			
*Direction is given in Shuttle coordinate system				

3.2 ELECTRICAL CONFIGURATION

3.2.1 ELECTRICAL INTERFACES

3.2.1.1 Power

Due to the large repetitive current surges required by the Scatt Transmitter, separate input power busses are required. The baseline Scatterometer design (represented by the ROM cost of section 8.0) can accomodate the following interface requirements. Additional requirements such as source failure transients or other long term transients (>50 ms duration) imply changes to the design and may incur some additional costs above the baseline.

3.2.1.1.1 +28 VDC Main Bus (Regulated Bus)

DC Voltage:	+28 \pm 0.56V.
Source Impedance	0.3 ohms max for DC to 100 KHz.
Ripple:	100 mv p-p max for 100 Hz to 100 KHz.
Switching spikes:	1.0 mv peak max 1 μ max Duration 50,000 pps max rep rate
Power Consumption Average:	142W max (108W Typical)
Power Consumption (Peak):	165W max (128 Typical)
Load Current Ripple:	2% of Ave. Current
Load Current Transients: (The peak power specified above represent repetitive current surges during power strobing of circuitry)	+20% Max. of Ave current 20 ms max duration of peak 7% max Duty Cycle 100000 A/sec max di/dt
In rush current @ turn-on:	2 times max normal current 100,000 A/sec max di/dt

3.2.1.1.2 Pulse Load Bus

DC Voltage:	+28 \pm 4 VDC
Source Impedance:	0.3 ohm max for DC to 100 KHz
Ripple:	500 mv p-p max for 30 Hz to 1 MHz
Voltage Spikes:	4v peak max for 10 ms max
Power Consumption: Average:	110W max (20 W Typical)
Peak for 28 \pm 0.56V input:	309W max (252 W Typical)
Peak for 28 \pm 4V input:	334W max (272 W Typical)
(Note that peak currents are higher as the input voltage deviates more from the nominal)	
Load Current Transients: (includes turn-on in rush current)	14A peak max 100,000 A/sec max di/dt 5 ms nominal duration 16 ms nominal rep. period
Load Current Ripple:	8A peak max 100,000 A/sec max di/dt Variable duty cycle 10 to 50 KHz fundamental Frequency

3.2.1.1.3 Switched Telemetry Bus

The Scatterometer can accept an isolated Switched Telemetry Bus voltage to be used for temperature monitors.

3.2.1.1.4 Interface Power Bus

If required, the Scatterometer can accommodate an Interface Power input of 10 ± 0.5 VDC for powering the interface circuits. Alternatively, the Scatterometer could generate its own isolated power for interface circuits.

3.2.1.2 Grounds

The Scatterometer can maintain 100K ohm isolation between all grounds except that the Signal and Chassis grounds must be tied together (Note that the Signal Ground need not interface with the Spacecraft if an interface ground is used. Signal ground is defined as the secondary ground of the DC/DC converter of the Scatterometer).

If an isolated interface ground is required the potential between this ground and the chassis ground must be kept to less than ± 0.5 volts.

3.2.1.3 Input Commands

It is anticipated that the Scatterometer will require the following commands:

1. SCAT ON - Power up all functions except HVPS
2. HVPS ON - Power up High Voltage Power Supply if SCAT ON was previously sent
3. HVPS OFF - Power down HVPS
4. SCAT OFF - Turns off all functions, including HVPS, except heaters.
5. HEATER ON - Turns on heaters unless SCAT ON cmd has turned the on
6. HEATER OFF - Turns off heaters
7. STANDBY
MODE CMD - Turns off high voltage to TWT (no transmit pulses) all other functions as in normal operating mode.
8. Continuous
Cal Mode - Noise only and Noise + reference signal data taken continuously (no transmit pulses)

9. Operating Modes

- Normal operating modes. Some candidates are:

- a. Both sides @ 25 Km cell size
- b. Left Only } at 12.5 km in-track
- c. Right Only } all size

3.2.1.3.1 Discrete Commands

For commands 1 thru 6, above, it is recommended that the commands be 28v pulses of approx 60 ms duration to activate latching relays directly. This facilitates isolation of command return from other grounds.

3.2.1.3.2 Impulse Commands

For commands 7 thru 9 logic level commands are recommended. If an isolated +10v interface bus is used the logic levels should be +10 \pm 0.7V and 0 \pm 0.2 volts. Even without an isolated bus the 10v CMOS compatible logic levels will give better noise immunity than TTC levels. The commands could also be referenced to Signal Ground if zero isolation between Signal Ground and chassis ground is acceptable. The commands can be pulse type where the last command sent will determine the Mode of operation; or levels if the sender assumes responsibility for making only one command true at any given time.

3.2.1.4 Input Signals

The Scatterometer could require the following input signals:

1. Orbit Reference Marker - used to calculate latitude for co-registration. Could occur at equator crossing or some other constant point in the orbit.
2. Time Code - To time tag data, also may be used for latitude calculation.
3. Data System Timing Signals - If the Scatterometer is to be synchronized to the Data Subsystem a clock and synch signals will be required. A clock for shifting and data and a data enable signal may also be required.

Voltage levels for these signals could be 10V CMOS levels (10 \pm 0.7V High State, 0 \pm 0.2V Low State) or TTL levels. Isolated return could be accommodated if it is guaranteed to stay within \pm 0.5V of signal ground. Signal Ground could be used on the return if lack of isolation between Signal and Chassis Grounds is acceptable.

3.2.1.5 RF Clock

The Scatterometer contains its own stable clock reference for generating RF power and no external clock is required.

3.2.1.6 Data Interface

The baseline design (represented by the ROM cost of section 8.0) consists of the Scatterometer sending data to the spacecraft as a function of its own internal timing and asynchronously with the spacecraft Data Subsystem. The data could be sent in a burst once for antenna dwell period, or continuously. The average data rate will be less than 3 KBS.

The interface consists of three signals:

1. Serial Data
2. Data Clock
3. Data Valid Signal (burst Mode)
or
Frame Start Pulse (Continuous mode)

These signals all originate in the Scatterometer and no acknowledge or the "handshaking" responses are required or accepted from the spacecraft.

3.2.1.6.1 Data Format

The Data Frame (occurring once for Antenna dwell period) is transmitted on a single line in bit serial fashion and can be organized into 8, 10 or 16 bit words depending on spacecraft requirements. There is no word clock and the bits will have to be counted at the receiving end to permit breaking the frame into words. A typical frame would consist of:

32 to 40 bits of synch pattern.

Approx 100 bits of Bi-level Status Info and Time Cods

25 words (50 for 8 bit words) of Signal + Noise Data

25 words (50 for 8 bit words) of Noise only data

Approx 40 words of Analog Calibration and Housekeepig TLM Data

TBD space words

3.2.1.6.2 Timing

The timing of the Data, Clock and Data Valid signals can be accommodated to the spacecraft requirements. One clock cycle is required to shift out one bit of data. Data Valid goes TRUE before data during starts and goes FALSE after data during ends.

3.2.1.6.3 Signal Characteristics

Single ended CMOS levels ($+10 \pm 0.7V$ High state, $0 \pm 0.2V$ Low state) or dual complemented TTL levels (e.g. from a DM7830 line driver) are recommended. Isolated power and ground for these signals can be accommodated provided the potential between this return and Scatter signal ground is maintained at less than ± 0.5 volts.

3.2.1.6.4 Alternate Data Interface

If it is required that the spacecraft read the state (instead of the Scatterometer dumping the data whenever it is ready) it will be highly desirable to synchronize the Scatter timing to the data system timing. This option, with or without synchronization, is more costly than the baseline approach.

3.2.1.7 Telemetry Interface

Analog temperature telemetry data is derived from resistor/thermistor networks across the Switched Telemetry Bus and its return. The Telemetry is referenced to the Switched TLM Bus Return and maximum Signal level is determined by the Bus voltage. Output impedance and noise suppression can be accommodated to TLM subsystem requirements.

Bilevel telemetry of relay functions are available. They are derived by placing a space relay contacts in series with resistors across the Switched TLM Bus and its return so that Low State is a short to the S.W. TLM Bus Return and High state is the S.W. TLM Bus voltage thru a resistance of TBD ohms.

3.2.1.8 Connectors

Separate connectors will be provided for Power, commands/inputs, data output, Telemetry, and test points.

All test points will have series resistors to protect the Scatterometer circuitry from shorts to ground or application of voltage of up to $\pm 28V$.

3.2.2 ANTENNA DESIGN

3.2.2.1 Antenna Fields-Of-View

Requirements for the antenna fields-of-view and orientation will be defined for the six (6) antennas of the Antenna Assembly so as to satisfy the Scatterometer coverage and pattern requirements for the NROSS Scatterometer System. The desired footprints of the Scatterometer antenna patterns on the surface of the Earth are shown in Figure 3.2.2-1.

The angles from Nadir to the 176 km and 776 km swath edges are about 17.7° and 53° for the $\pm 45^\circ$ footprints (#1, 3, 4 and 6), and 13.2° and 46° for the $+65^\circ$ and -115° footprints (#2 and 5), for a nominal 830 km orbit height. The individual antennas will thus be rotated about their axes about 35° and 30° so as to illuminate the desired footprints with the broad-beam patterns.

One basic arrangement of the antennas for achieving the desired footprints with minimum beam interference by the antennas is shown in Figure 3.2.2-2. The peak of the narrow-beam pattern is nearly broadside to the waveguide array with a small squint angle θ_s of about 2° , thus the broad-beam pattern of Antenna #1 produces a footprint at $+45^\circ$ when the antenna is oriented at about $+133^\circ$ as shown, and similarly for the other antennas.

More compact alternative arrangements can be obtained by effectively sliding antennas diametrically across to form a back-to-back arrangement, as shown in Section 3.1.2.3.

The broad-beam pattern actually lies along a shallow cone of about 88° half-cone angle, rather than in a plane. The orientation of Antenna #1, for example, would thus be attained by first orienting the antenna at $+135^\circ$ with the beam pointing toward Nadir, rotating the antenna 35° about its axis toward $+45^\circ$, and then tilting the antenna about 2° in the 35° plane to correct for the squint angle. The other antennas would be oriented in a similar manner. The tangent plane to the broad-beam pattern would thus lie along the centerline of the footprint at the beam peak and would gradually curve away toward the edges of the swath. This departure from a straight-line footprint can be corrected in the data processing algorithms.

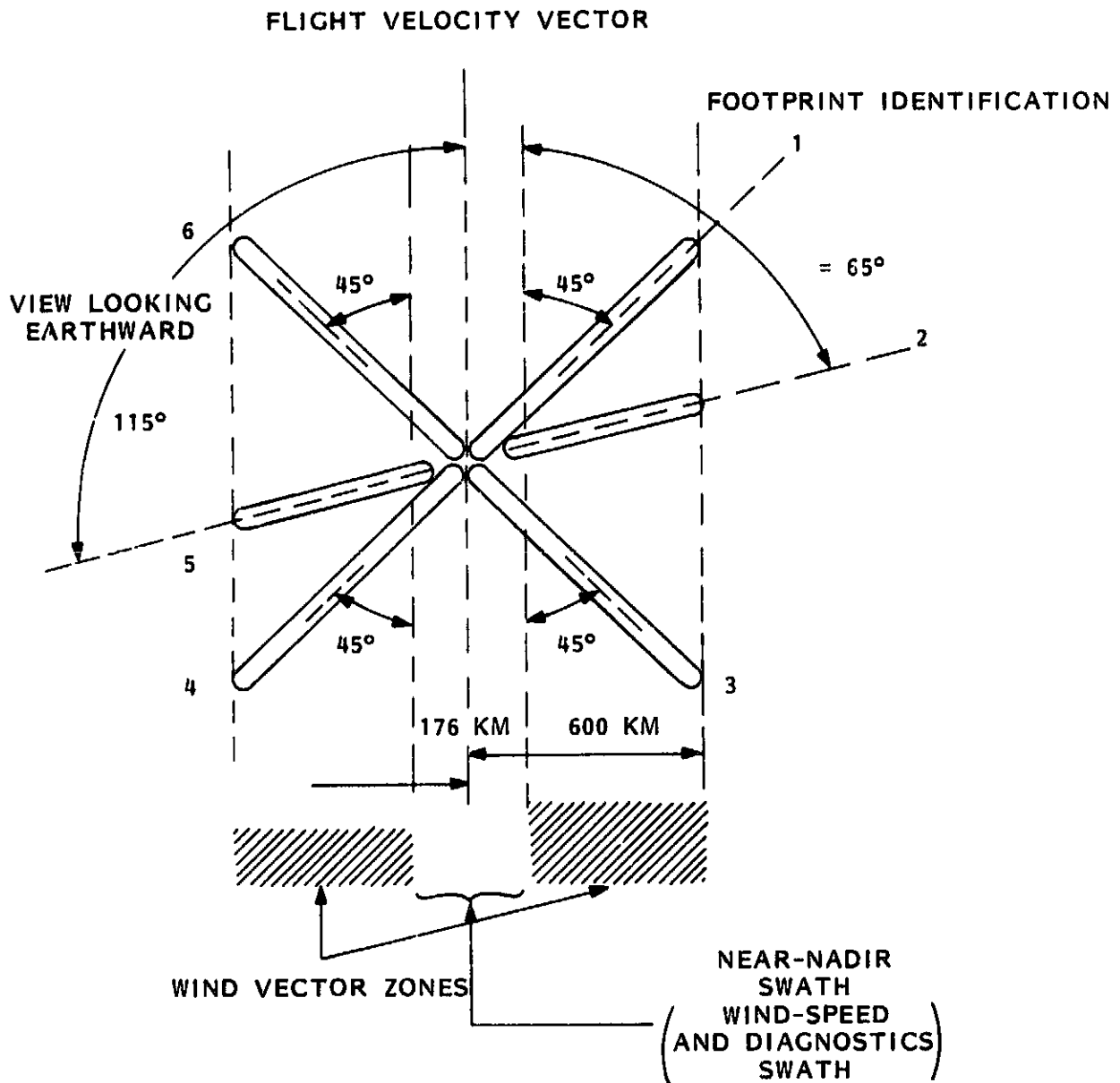


Figure 3.2.2-1. Scatterometer Antenna Footprints on Earth

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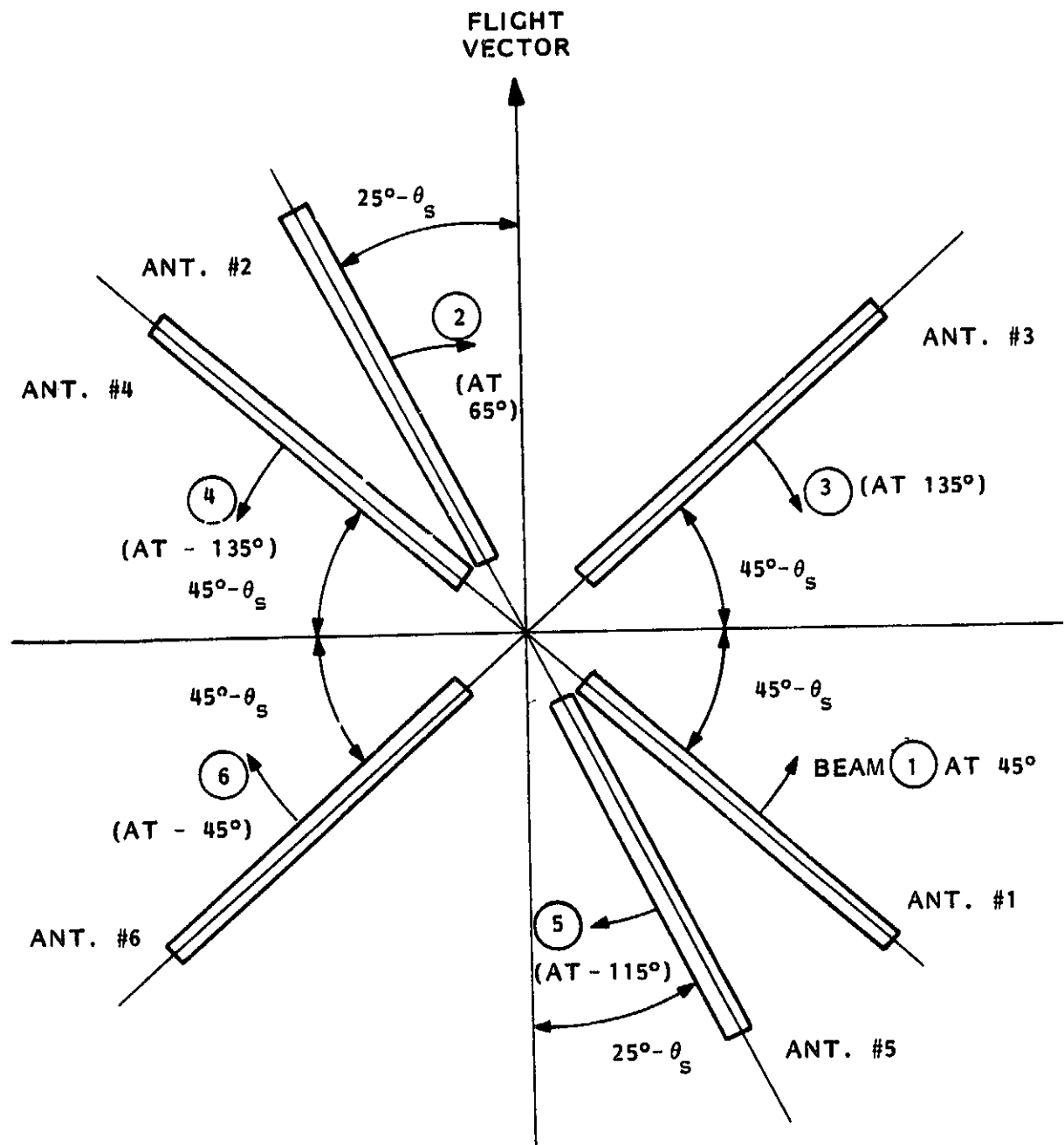


Figure 3.2.2-2. Basic Arrangement of NROSS/Scatterometer Antennas for Minimum Beam Interference as Viewed From Spacecraft Looking Toward The Earth

3.2.2.2 Engineering Model Antenna

The Scatterometer Antenna Assembly consists of six linearly polarized antennas that are pointed in six different azimuthal directions and inclined Earthward for the same nominal Earth incidence angle. Each antenna consists of an array of three waveguide slot arrays mounted on a support member. Four of the antennas are polarized vertically (#1, 3, 4 and 6), and two are polarized horizontally (#2 and 5). The pattern of each antenna is fan-shaped with a narrow azimuthal beamwidth.

The antenna configurations that are proposed are essentially identical to each half of the dual polarized antennas that were successfully flown as part of the Seasat A Satellite Scatterometer (SASS) System. A photograph of that antenna is shown in Figure 3.2.2-3. The primary differences between the individual SASS and NROSS/Scatterometer antenna results from the change in the center frequency of the two systems. At 13.995 GHz, the length of the NROSS/Scatterometer antenna is approximately 109.6 inches, or 4.7 inches longer than the 14.59927 GHz SASS Antenna.

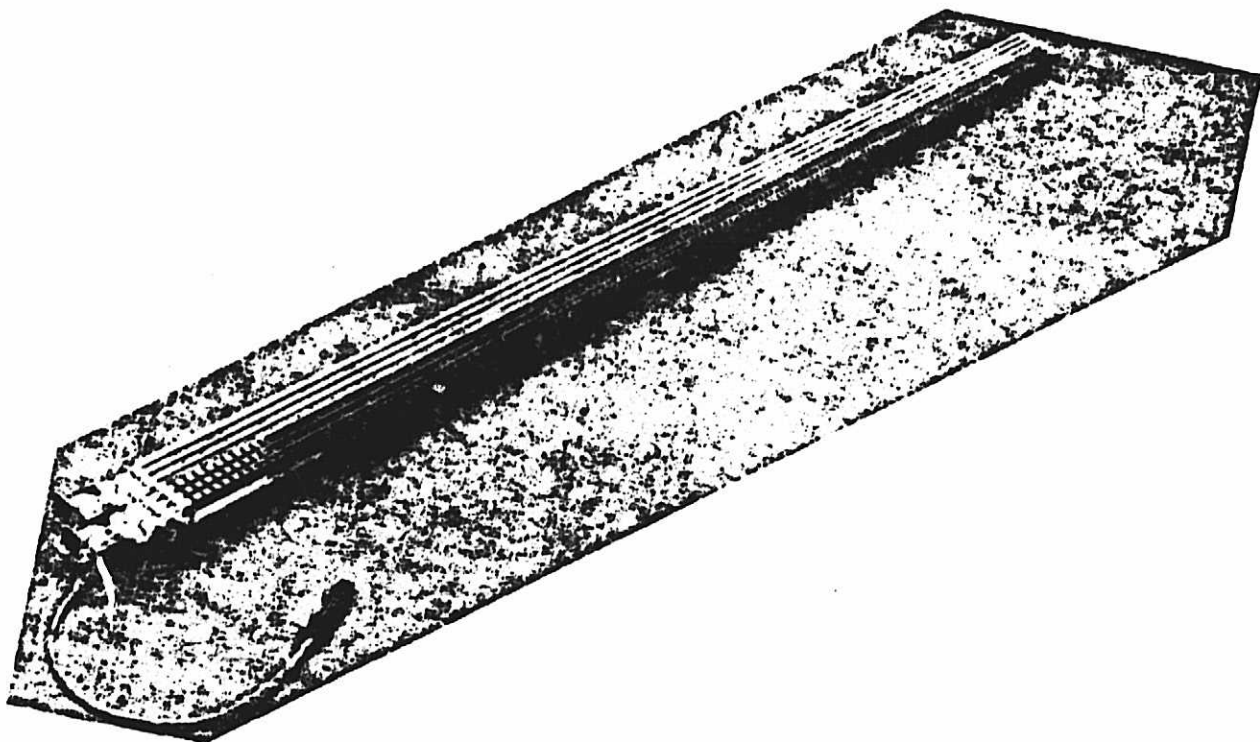


Figure 3.2.2-3. Seasat A Scatterometer (SASS) Antenna

3.2.2.2.1 Antenna Specifications

The primary RF and mechanical specifications for each antenna of the Antenna Assembly are summarized in Table 3.2.2-1.

3.2.2.2.2 Design Description

Two separate linearly-polarized slotted waveguide phased arrays each mounted on a support member, comprise the antenna system. The design of both arrays is similar, with three waveguides having 138 slots each for both arrays. Broadwall slots are used in one array to achieve vertical polarization and edgewall slots in the other for horizontal polarization.

Waveguide corporate feeds are used to excite each array so as to form the fan beam. The feeds are physically identical except that a set of twists are utilized to mate the corporate feed with the edgewall slotted array. Each element of the array is a traveling wave type with a 30-dB sidelobe Taylor amplitude distribution design. The element provides collimation in the narrow-beam plane. This approach is a simple means of illuminating the aperture and is characterized by a low input VSWR and relatively low loss. This method of power distribution, however, requires that a small percent (5%) of the input power be terminated in a step load at the end of each waveguide element. In order to achieve a low input VSWR, a nominal beam tilt of 2° is incorporated into the aperture design. In spacing each slot in the array to achieve this beam tilt, the reflections from each slot tend to cancel and thereby produce the desired low VSWR.

Baffles are inserted on each side of the broadwall slotted array elements to provide a more directive slot pattern in the broad-beam plane of the array and also to reduce any mutual coupling effects across the array. Baffles are not required for the edgewall slotted configuration since the slot characteristics are already fairly directive in the broad-beam plane and the mutual coupling across the array is small.

Table 3.2.2-1. Antenna Specifications

<u>RF SPECIFICATIONS</u>	
Center Frequency	13.995 GHz
Bandwidth	± 1 MHz
Beam Tilt from Broadside	$\geq 2.2^\circ$
Nominal Beamwidth	$0.5^\circ \times 25^\circ$
Polarization	Linear vertical/horizontal
Gain (Peak)	≥ 32.5 dB Above Isotropic
($+18.5^\circ$ from Beam Center in Broad-Beam Plane)	≥ 24.5 dB Above Isotropic
($+24^\circ$ from Beam Center in Broad-Beam Plane)	≥ 20.0 dB Above Isotropic as a Design Goal
Gain Slope ($+18.5^\circ$ from Beam Center in Broad-Beam Plane)	≤ 1.1 dB/Degree
Gain Characteristics (30° to 40° and -30° to -40° from Beam Center in Broad-Beam Plane)	≤ 15 to 18 dB Below Beam Peak as a design goal
($+42^\circ$ from Beam Center in Broad-Beam Plane for At Least One Polarization)	≤ 21 dB Below Beam Peak With ≤ 19 dB as a Design Goal
Peak Cross-Polarized Lobes	≥ 20 dB Below Beam Peak
Sidelobe Level:	
Broad-Beam Plane	> 12 dB Below Beam Peak Beyond $+42^\circ$
Narrow-Beam Plane	> 20 dB Below Beam Peak
Spurious Lobes:	
$\theta \geq 32^\circ$ from Beam Peak (Narrow-Beam Plane)	> 18 dB Below Beam Peak
$\phi \geq 36^\circ$ from Beam Peak (Broad-Beam Plane)	> 18 dB Below Beam Peak

Table 3.2.2-1. Antenna Specifications (Cont'd)

$\theta < 32^\circ$ from Beam Peak (Narrow-Beam Plane)	>14 dB Below Beam Peak
$\phi < 36^\circ$ from Beam Peak (Broad-Beam Plane)	>14 dB Below Beam Peak
All other Spurious Lobes	> 20 dB Below Beam Peak
Maximum Variation in Beam Pointing Direction in Orbit	$\pm 0.75^\circ$ and Predictables to $\pm 0.2^\circ$
Maximum RF Input Power Levels	135 Watts Peak (5 MS Pulse width and 55-65 PPS Repetition Rate)
Input VSWR	$\leq 1.3:1$
Waveguide Input	WR62 Waveguide with UG-419/U Cover Flanges
<u>MECHANICAL SPECIFICATIONS</u>	
Maximum Envelope	320CM X 12CM X 12CM
Maximum Weight	30 LBS
Minimum Natural Frequency	18 Hz
Minimum Cantilever Natural Frequency	1.5 Hz

The array elements are made from special tolerance WR-51 aluminum waveguide. The corporate feeds have a WR-62 waveguide input and WR-51 waveguide outputs with special narrow-width flanges. The use of a complete waveguide approach to the aperture design yields a configuration with a simple means of aperture illumination control within a relatively low loss and well matched package.

Structural support and stiffness is provided by WR-137 aluminum waveguides bonded between two sheets of 0.127 cm (0.050") thick aluminum. This simple sandwich structure provides an extremely stiff and stable mounting base and is fabricated with standard waveguide extrusions. A forward and rear support are mechanically attached and bonded to the structure and are the mounting interfaces to the sensor module. Brackets are also incorporated at both the forward and rear supports to transfer loads to the sides of the antenna.

Both silvered Teflon and white thermal paint are used for passive thermal control to reduce front-to-back thermal gradients that produce undesired antenna distortion. A set of ten temperature thermistors are mounted along the length of the antenna to measure front-to-back thermal gradients generated under orbital conditions. The thermistors are wired to a common output connector. Protective covers bonded to the sides of the antenna shade the thermistors and the thermistor cable from the Sun. Silvered Teflon is attached to the outside of these covers.

3.2.2.2.3 Design Detail

Linear Array Element. Both the broadwall and edgwall arrays use resonant length slots that are alternately inclined to provide the coupling that results in the desired aperture illumination. Slot resonant length data at the operating frequency and slot coupling data as a function of inclination angle for both the broadwall and edgwall configuration are obtained experimentally using test sections made up of thirty slots each. These data are then used in the design of a half-size and a full-size brassboard model. Characteristics of both the broadwall and edgwall full size linear array elements are as follows:

Aperture Illumination	30 dB sidelobe, Taylor ($\bar{n} = 4$)
Aperture Size	109.65 inches
Number of Slots	138
Slot Spacing	0.800 Inch
Power Dissipated in Load	5%
Waveguide Size	WR-51

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Corporate Feed. The waveguide corporate feed provides three output ports from a common input port with the power level at each port controlled by power dividers of a special H-plane design. Phase relationships at the output ports are controlled by the overall electrical length from the input port. In this design the power split is governed by the offset of a septum from the centerline of the input waveguide; the input impedance is matched by irises and the relative phase of the output arms is balanced by a short section of waveguide that is narrowed in the broad dimension. Corporate feeds mounted on a brassboard model are shown in Figure 3.2.2-4. Characteristics of the corporate feed design are as follows:

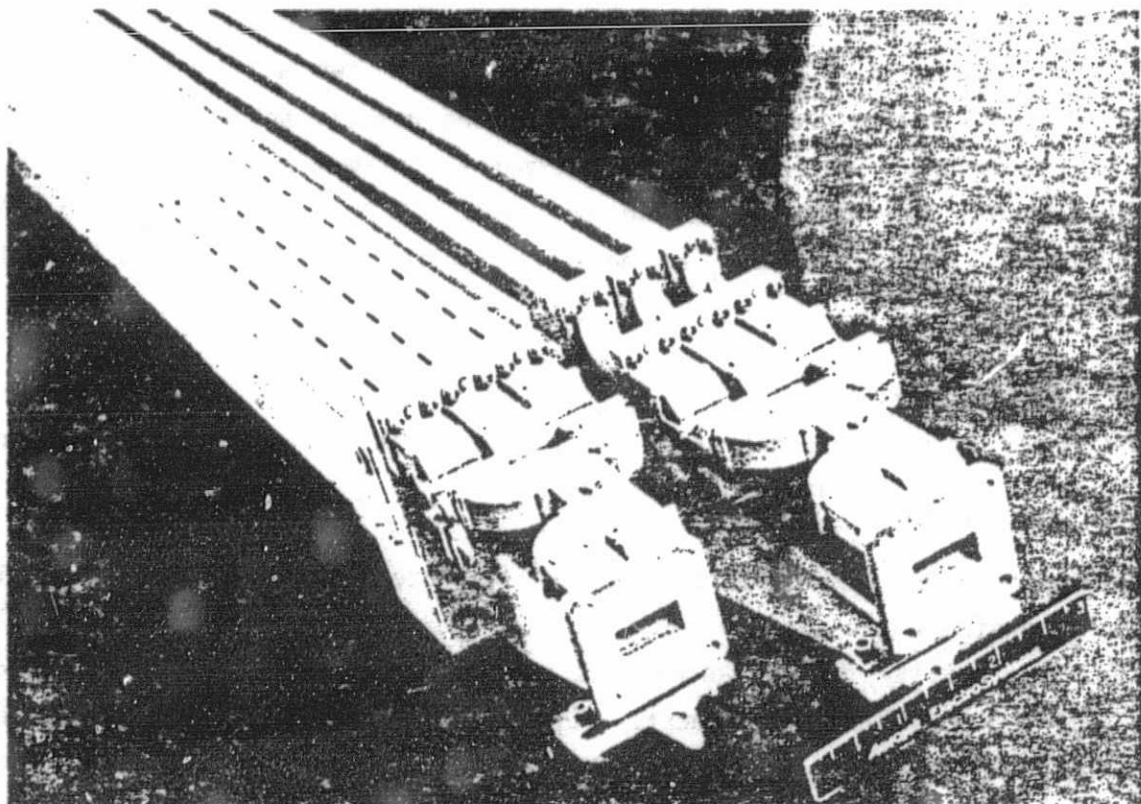


Figure 3.2.2-4. Feeds Mounted on Brassboard Model Antenna

Number of Output Ports	3
Port-to-Port Spacing	0.678 inch
Output Waveguide Size	WR-51
Input Waveguide Size	WR-62
Relative Voltage Distribution	0.553, 1.00, 0.553
Phase Distribution	-28°, 0°, -28° (broadwall array) -30°, 0°, -30° (edgwall array)
Input VSWR	≤1.15:1
Loss	≤0.25 dB

Load Termination. A single-step load design is used for the end termination. This load is fabricated out of a metal-loaded epoxy material that provides the required RF absorbing medium.

3.2.2.2.4 Antenna Performance

During the design phase of the program antenna performance characteristics such as patterns, gain, impedance and power handling capability will be calculated. Results of these calculations will be compared with measurements made on a full-size brassboard antenna. It is expected that the two will compare quite favorably with one another and will approximate the results achieved previously with the SASS Antennas. Typical of the performance achieved previously with the SASS Antenna design are the data shown in Table 3.2.2-2 and Figures 3.2.2-5 through 3.2.2-10. These data are as measured on SASS Flight Antenna Serial Number A-5.

3.2.2.3 Flight Model Antenna

The Flight Model Antenna Assembly will be identical in design, materials, and construction to the Engineering Model Antenna.

One FM Antenna of each polarization will be subjected to qualification level testing to demonstrate the overall integrity of the RF, structural and thermal designs and the ability of the antenna to survive the launch environment and function in the orbital environment. Upon successful completion of the qualification level testing, the remaining four antennas of the FM Antenna Assembly will be subjected to acceptance testing to verify the workmanship in these antennas.

Table 3.2.2-2. Typical SASS Antenna Performance (S/N A-5)

TEST PARAMETER	SPECIFIED VALUE	PRE-ENVIRONMENTAL MEASURED VALUES		POST-ENVIRONMENTAL MEASURED VALUES	
		BROADWALL (VERT. POL.)	EDGEWALL (HORIZ. POL.)	BROADWALL (VERT. POL.)	EDGEWALL (HORIZ. POL.)
1. POLARIZATION ORIENTATION VERT. 0° HORIZ. 90°		0°	0°	0°	0°
2. PEAK GAIN GAIN 18.5° FROM BEAM CENTER IN WIDE-BEAM PLANE	≥ 32.5 dBi	33.5 dBi	32.5 dBi	33.5 dBi	32.5 dBi
3. GAIN FUNCTION (VERTICAL POLARIZATION ONLY) 12° TO 39.5° FROM BEAM CENTER IN WIDE BEAM PLANE	≥ 29.5 dBi 15 TO 19 dBi	25.9 dBi 25.6 dBi 18.5 TO 18.7 dBi 18.5 TO 18.8 dBi	25.5 dBi 26.0 dBi 10.3 TO 10.6 dBi 12.3 TO 12.3 dBi	25.9 dBi 26.2 dBi 10.9 TO 19.1 dBi 12.9 TO 19.0 dBi	25.2 dBi 25.5 dBi 10.9 TO 18.9 dBi 12.3 TO 12.9 dBi
4. GAIN SLOPE (18.5° FROM BEAM CENTER IN WIDE BEAM PLANE)	< 21 dBi BELOW BEAM PEAK	19.8 dBi 18.7 dBi	11.2 dBi 12.5 dBi	19.8 dBi 19.7 dBi	11.6 dBi 12.5 dBi
5. PEAK CROSS POLARIZED LOSS	< 1.1 dB/DEGREE	0.8 dB/DEG	0.7 dB/DEG	0.75 dB/DEG	0.7 dB/DEG
6. SLOTTED LEVEL (WIDE BEAM PLANE)	≥ 20 dBi BELOW BEAM PEAK	23.2 dBi	32.0 dBi	23.5 dBi	32.0 dBi
7. NARROW BEAM PLANE 12° FROM BEAM PEAK	> 12 dBi BELOW BEAM PEAK	18.5 dBi	10.7 dBi	18.9 dBi	10.9 dBi
8. HALF-POWER BEAM WIDTH (NARROW BEAM PLANE)	> 20 dBi BELOW BEAM PEAK	27.8 dBi	22.5 dBi	25.0 dBi	28.5 dBi
9. BEAM TILT FROM BROADSIDE (NARROW BEAM PLANE)	0.5° NOMINAL	0.51° ± 0.03°	0.48° ± 0.03°	0.51° ± 0.04°	0.48° ± 0.04°
10. BEAM TILT FROM BROADSIDE (WIDE BEAM PLANE)	0° TO 2.2°	1.9°	2.1°	1.9°	2.1°

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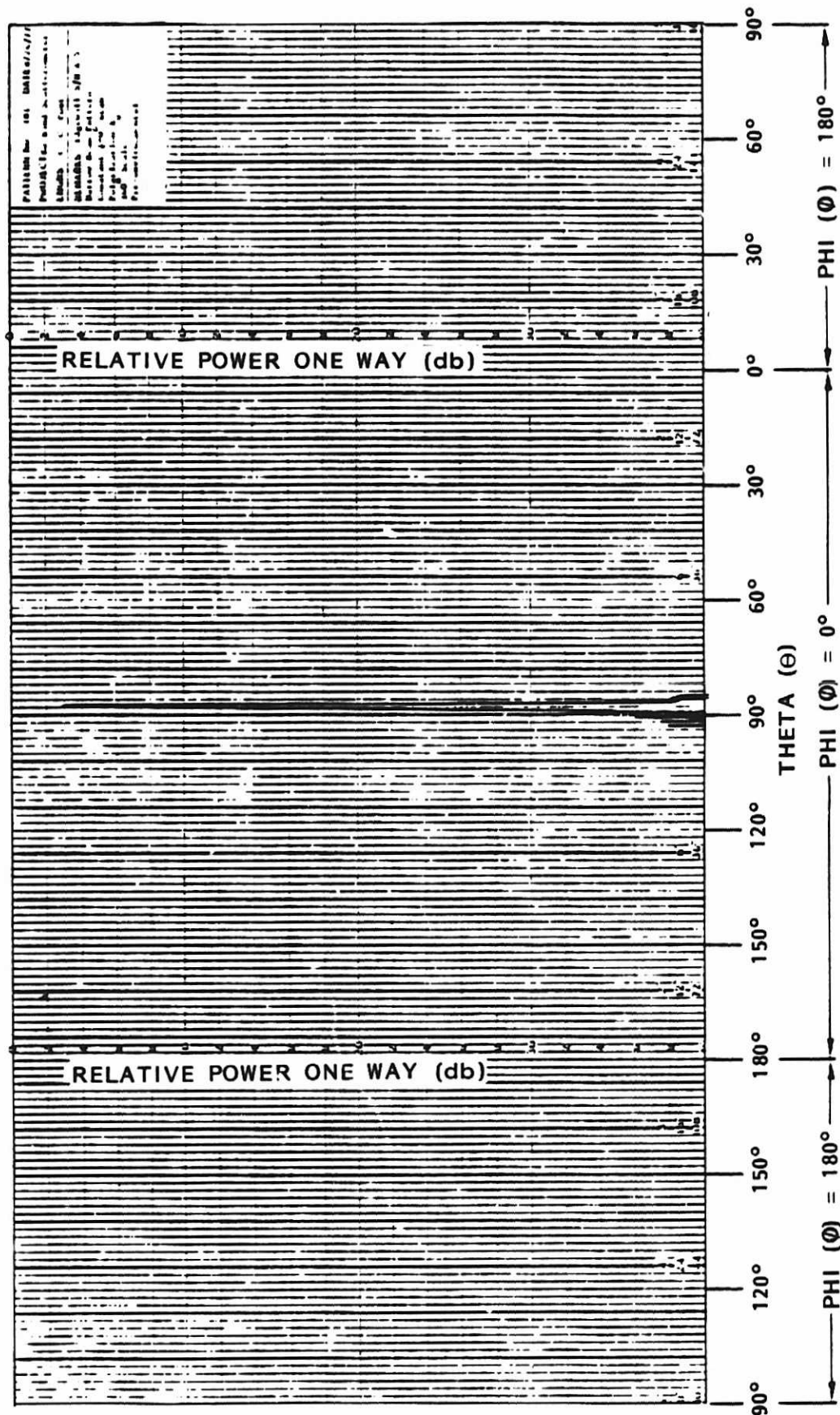


Figure 3.2.2-5. SA55 Antenna Pattern: Edgewall Array, Narrowbeam

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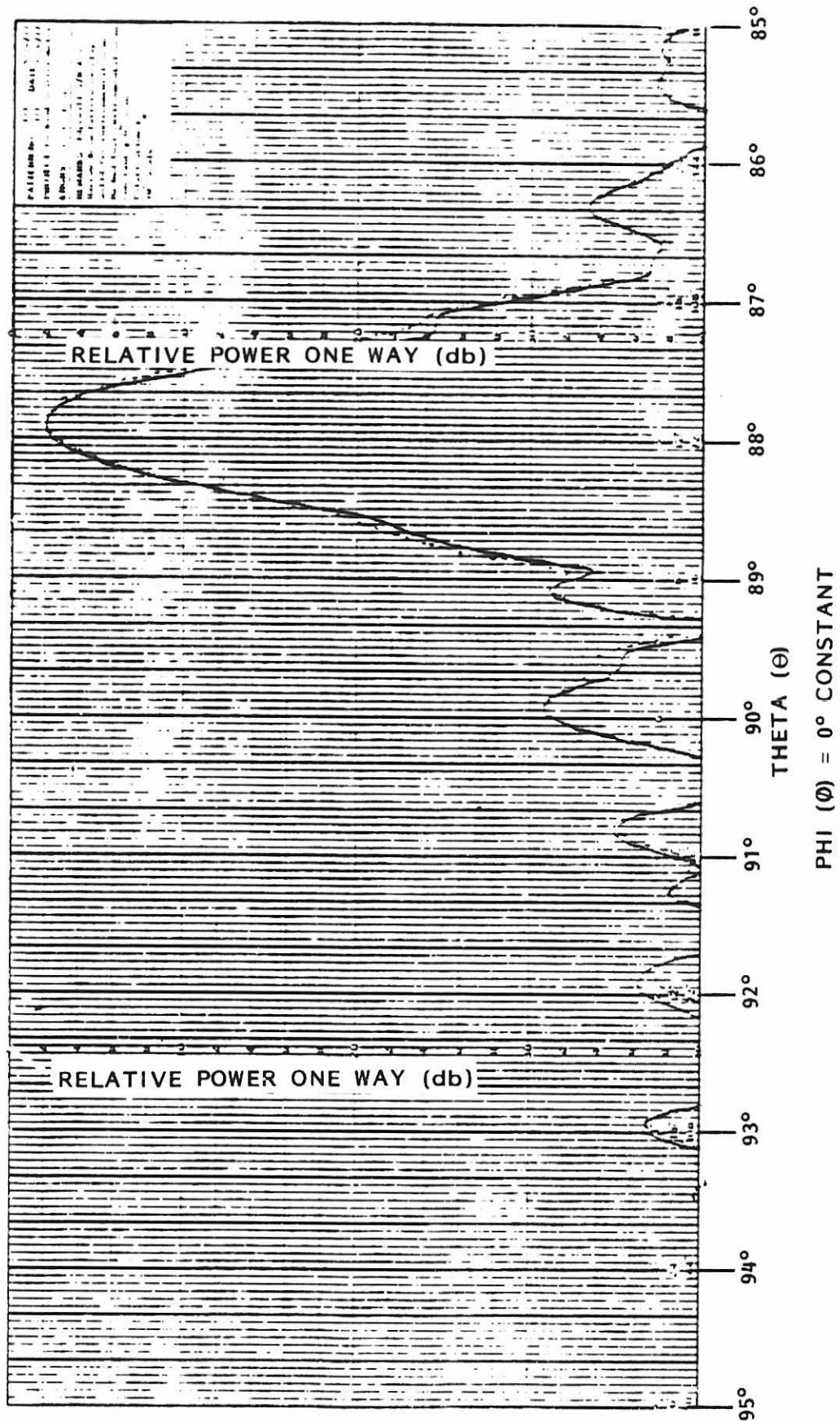


Figure 3.2.2-6. SASS Antenna Pattern: Edgewall Array, Narrowbeam (Expanded)

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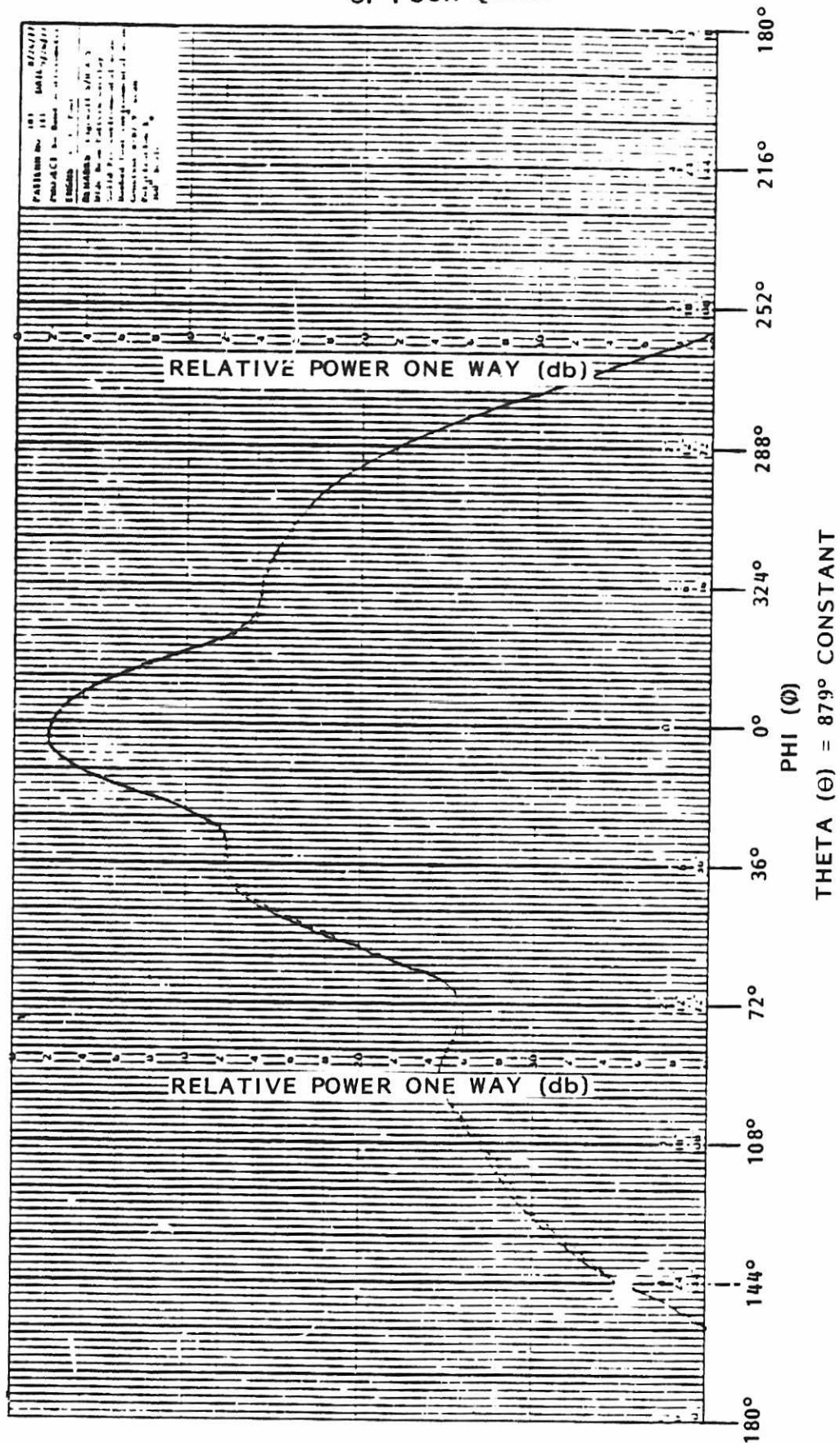


Figure 3.2.2-7. SASS Antenna Pattern: Edgewall Array, Widebeam

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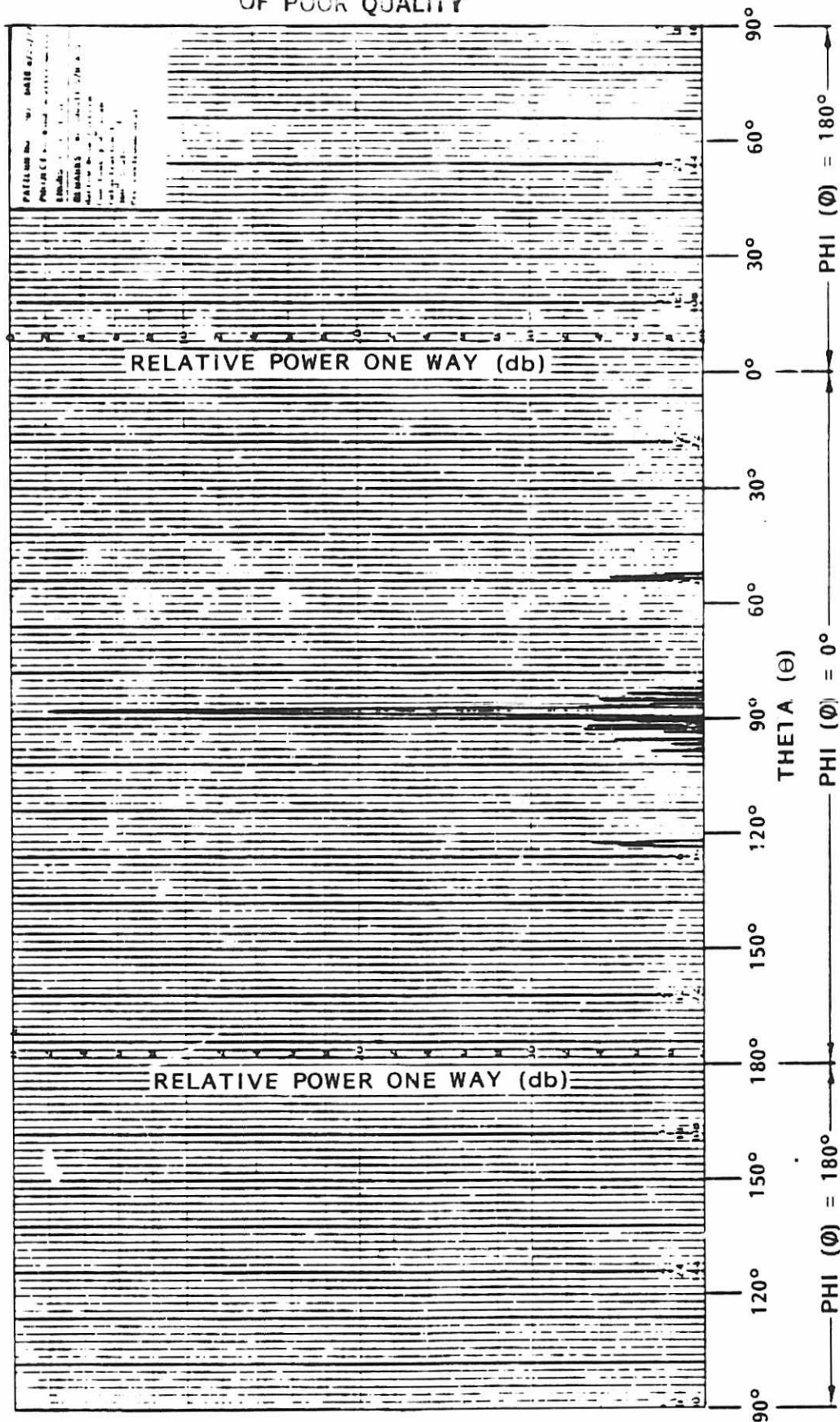


Figure 3.2.2-8. SASS Antenna Pattern: Broadwall Array, Narrowbeam

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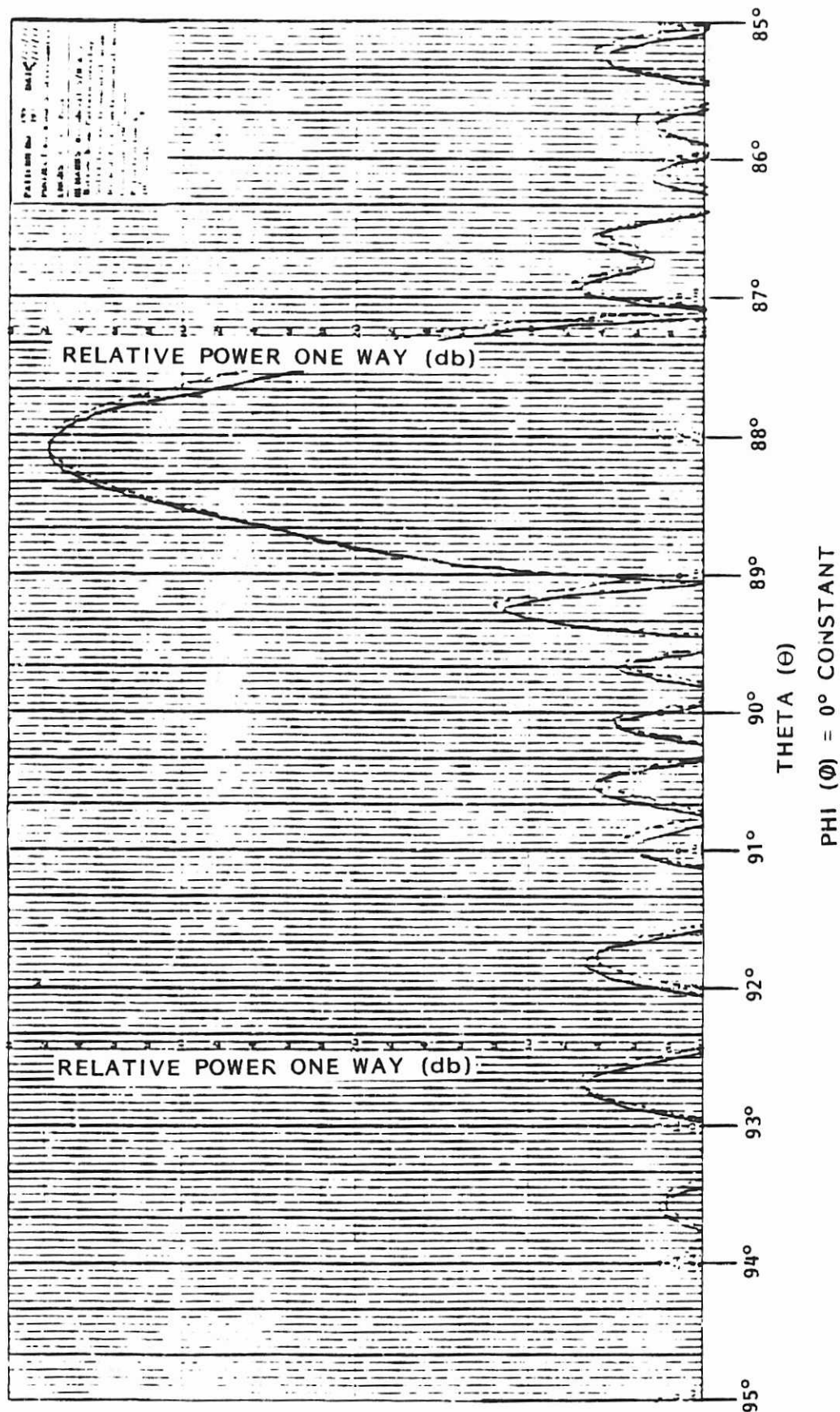


Figure 3.2.2-9. SASS Antenna Pattern: Broadwall Array, Narrowbeam (Expanded)

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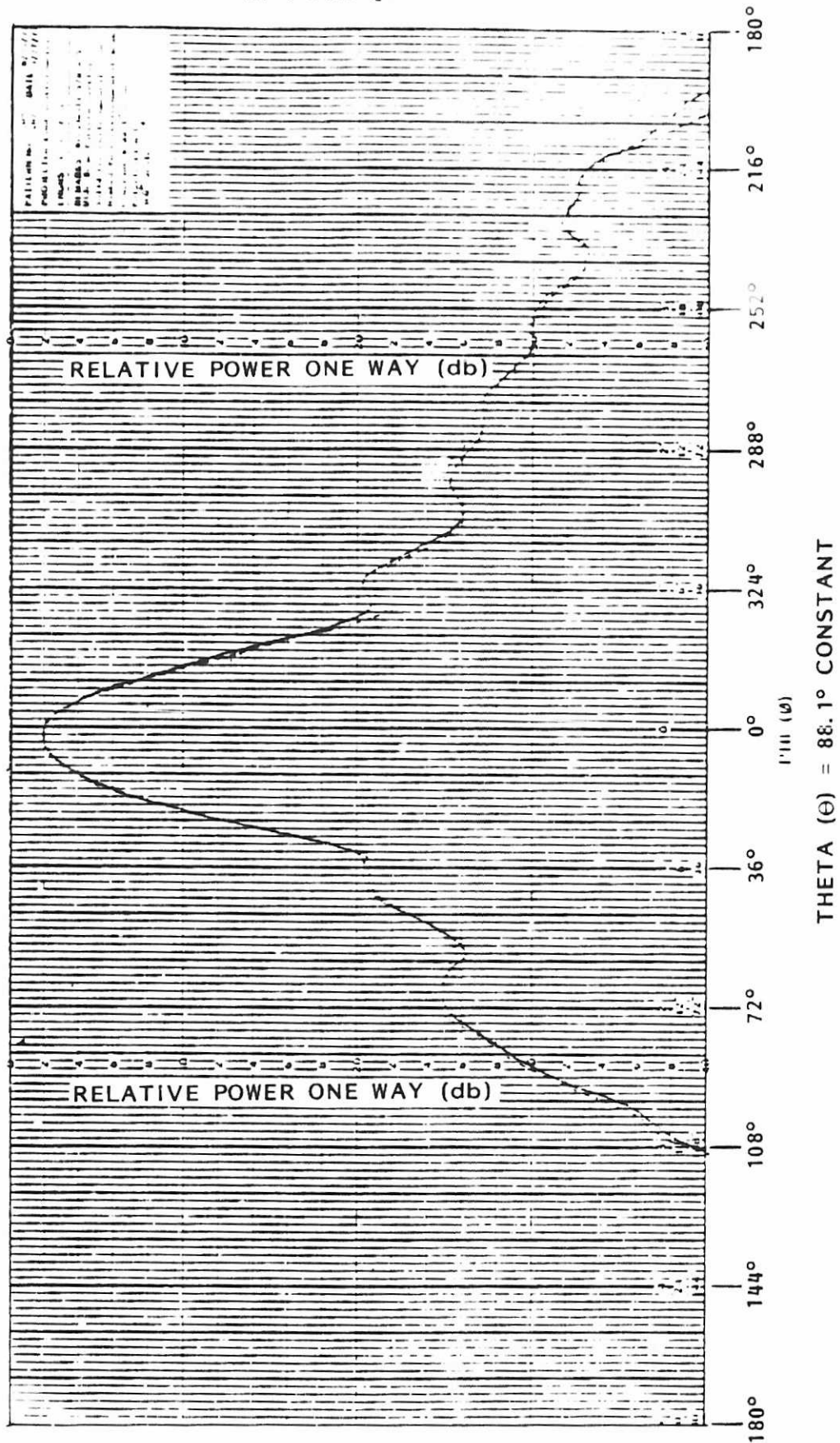


Figure 3.2.2-10. SASS Antenna Pattern: Broadwall Array, Widebeam

Antenna VSWR, isolation, peak power and thermal vacuum measurements will be made using AESC facilities. Shock, random vibration and acoustic measurements will be made at facilities in the Los Angeles area. Antenna pattern measurements will be made at the Physical Science Laboratory of the New Mexico State University in Las Cruces, New Mexico. Such facilities were used previously in the measurement of the performance of the SASS antennas.

3.2.3 TRANSMITTER

3.2.3.1 Frequency Sources

A block diagram of the proposed Scatterometer transmitter is shown in Figure 3.2.3-1. The basic transmitter design is the same as that used for Seasat A Scatterometer; however, the downconverter mixer has been changed to achieve higher reliability and the transmit Source Signal has been changed from 14.400 GHz to 14.192 GHz due to new frequency assignments for the NROSS Spacecraft. Improvement in system reliability will be obtained with the substitution of a double balanced mixer, which uses a diode quad, for the single diode mixer used in the Seasat A Program. The change in transmit frequency may require a modification to the bandpass filter's iris dimensions.

3.2.3.1.1 Frequency Source

A space-qualified crystal controlled 5 MHz frequency standard will be used as the prime frequency source for the NROSS Scatterometer. This highly reliable stable source is the same as that currently used by General Electric in the DSCS III Communications Satellite. This is a new item for NROSS; for SASS and NOSS a frequency reference was supplied by the spacecraft to the Scatterometer.

3.2.3.1.2 Solid State Source/Local Oscillator (SSS/LO)

The SSS/LO provides three RF signals for use as transmit carrier, transmit modulation, and switched Local Oscillator. These signals are coherently generated by the SSS/LO through multiplication or phase-lock techniques from the high stability reference source. The output frequency of the transmit carrier is 2880 times the reference input frequency (4.9278 MHz) or nominally 14.192 GHz (C.W.) with a 15.0 dBm minimum power level. A pulsed RF input, 40 times the input frequency or nominally 197.112 MHz, is provided at the transmit modulation

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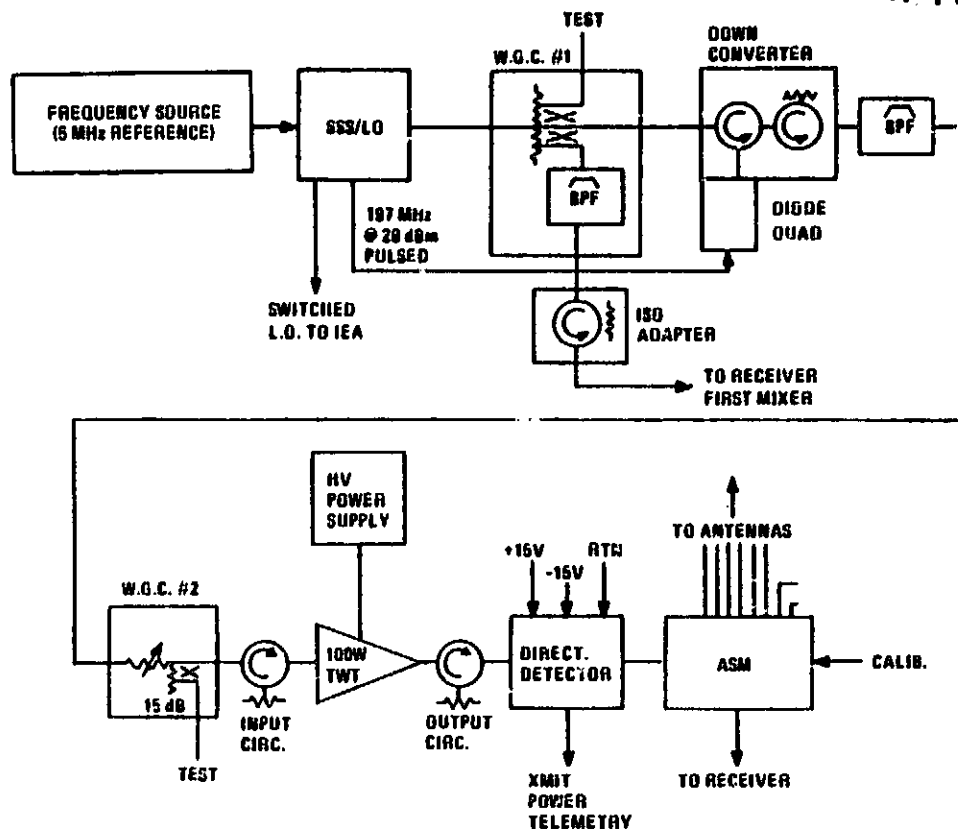


Figure 3.2.3-1. Scatterometer Transmitter Block Diagram

port. The Switched Local Oscillator (SLO) signal eliminates the need for a negative Doppler processing channel and is a single output which is command selectable to one of two frequencies, which are 186.899 MHz and 205.325 MHz.

3.2.3.1.3 Downconverter (Transmit)

The design of the Downconverter will be modified from that of the Seasat A Scatterometer. Improvement in system reliability will be obtained by substitution of a double balanced mixer for the single diode mixer used in the Seasat A Scatterometer upconverter. The diode quad mixer will operate with reduced conversion efficiency with inoperative diodes. This will not degrade the overall performance of the Scatterometer since the TWT will remain in saturation even with the reduced RF input level caused by the lower conversion efficiency of the downconverter. Note that this mixing function was on upconversion on SASS but is a downconversion for NROSS ($14.192 \text{ GHz} - 197.112 \text{ MHz} = 13.994888 \text{ GHz}$)

3.2.3.1.4 Traveling Wavetube (TWT)

The tube which will be used to obtain the required 100 Watts RF output power is derived from that designed for the Seasat A Scatterometer Program. Scaling the slow wave coupled cavity structure somewhat to achieve operation at 13.995 GHz should not cause any problems and no increase in cathode current density is expected. It is expected that the actual saturated gain will be about 46-48 dB with a minimum RF output power of 100 Watts at 13.995 GHz. The TWT will have a maximum output power ripple that is less than 0.5 dB peak-to-peak over the frequency band and will have adequate phase and group delay characteristics for the intended usage.

3.2.3.2 High Voltage Power Supply

The High Voltage Power Supply (HVPS) for the NROSS Scatterometer will provide the voltages and currents required by a high power, multi-staged depressed collector, grid modulated Traveling Wave Tube (TWT).

The design proposed and costed in section 8.0 is identical to that flown on the SASS program, in fact, it will be a "build to print" SASS HVPS and it was assumed that no analyses such as worst case, FMEA, part stress, etc will be required for NROSS since it is a flight qualified design. Furthermore, since test procedures for all levels of assembly are on file, no costs were included for test plans and procedures. Description of the design follows:

The Scatterometer pulsed operation characteristics place very tight performance specifications on the power supply and many unique and challenging requirements on the system. For example, the grid modulator circuits provide TWT cathode current modulation and must switch the grid voltage between +300V and -500V with respect to the -8KV cathode voltage; the pulsed operation implies that the cathode and collector supplies provide 250 watts during the transmission period and zero watts for the remaining portion of the approx 16 milli-second cycle; and the RF pulse shape requirements further imply the need for excellent transient response for the cathode voltage and rapid switching of the grid voltage.

3.2.3.2.1 TWT Description and TWT/HVPS Interface

Figure 3.2.3-2 shows the interconnection diagram of the TWT and HVPS with typical voltages and currents indicated for a TWT driven to RF saturation. With power applied to the tube and with the grid biased to the conduction state, an electron beam flows from the cathode to the collectors. As it passes through the slow-wave coupled cavity region, the beam interacts with the RF wave such that the kinetic energy of the beam is converted into electromagnetic energy, thereby, increasing the amplitude of the RF wave.

Electrons emerging from the coupled cavities enter the collector region. The collectors have three electrical functions: (1) to sort electrons according to their velocities; (2) to slow the electrons so they may be collected with the lowest possible kinetic energy, thus minimizing thermal dissipation and maximizing efficiency; and (3) to prevent back streaming of electrons into the tube circuit. Since the electron velocity spectrum varies dramatically with RF input level and frequency, the beam current division between the various collectors also changes while the total beam current remains constant, with no RF applied to the tube, nearly all of the electrons emerging from the cathode reach Collector 4, the most negative collector electrode (electrons have maximum velocity since minimal kinetic energy has been removed from the beam in the slow wave structure). This condition corresponds to minimum electrical input power for a tube biased to conduction. As RF is applied, more and more electrons are intercepted by less negative electrodes, increasing the electrical input power.

With the pulsed mode operation required by the Scatterometer, the characteristics become even more complicated. In order to meet the RF isolation and the ENR requirements during the receive portion of the measurement cycle, an aperture grid was incorporated into the TWT gun design. With the grid biased to "cut-off" no electrons are emitted from the cathode; i.e., the beam is cut-off and thus the HVPS's cathode and collector supplies deliver no power. With the grid biased to "conduction" the full beam current flows, regardless of the RF input conditions. Further, as the grid potential is switched from conduction to cut-off or vice-versa the beam is not well focused and a large amount of the current goes to the tube body. The beam current (I_K) and body current (I_W) characteristics are roughly as shown in Figure 3.2.3-3 as a function of the grid to cathode voltage (E_{gk}). The final complicating factor results from the fact that the RF

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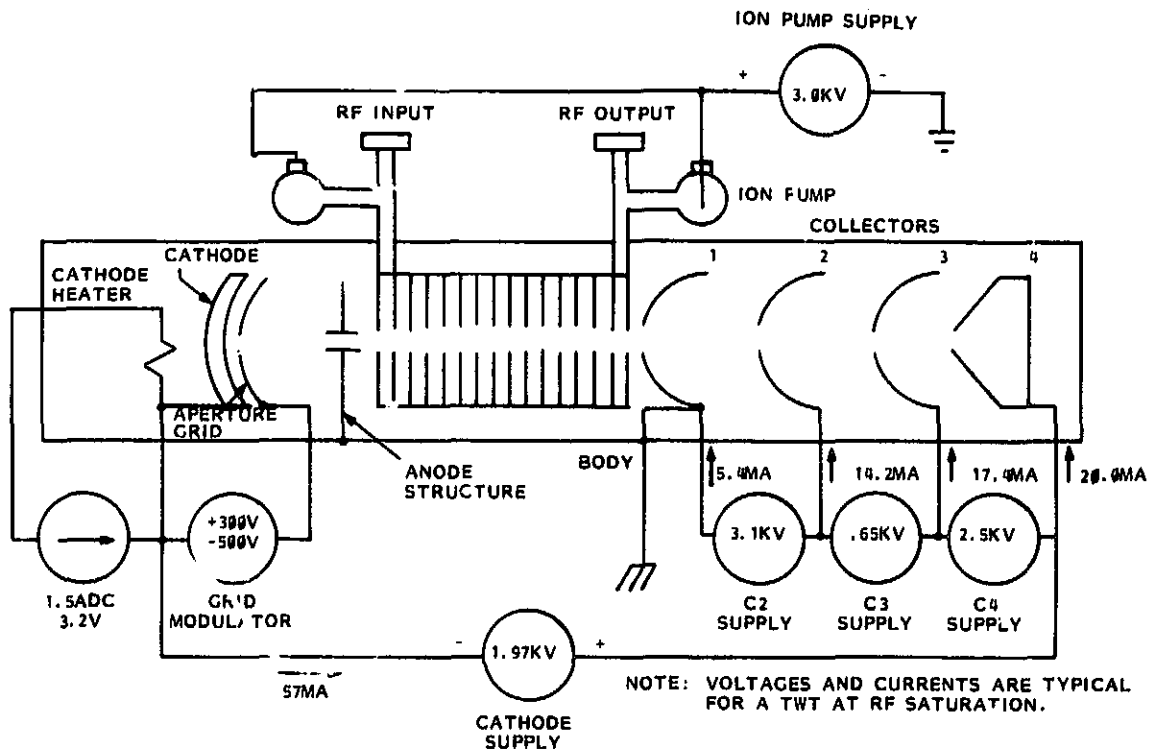


Figure 3.2.3-2. TWT/HVPS Interconnection Diagram

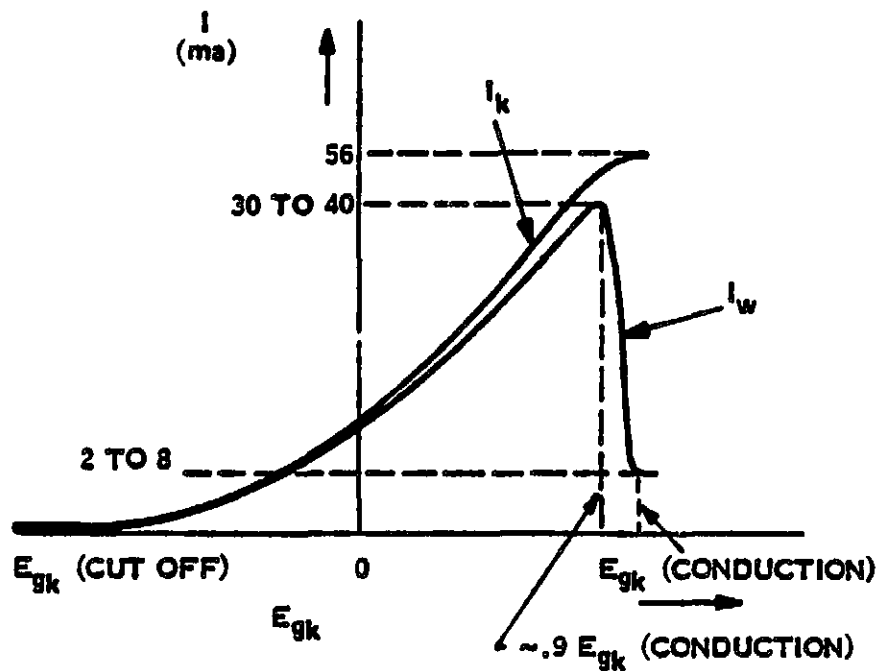


Figure 3.2.3-3. I_K and I_W VERSUS E_{GH}

is also pulse modulated and its timing is not coincident with the grid timing during turn on. Furthermore, each TWT is unique and each has its own set of interface characteristics. Resultingly, each HVPS is tailored to meet the requirements of a particular TWT with the primary change from unit to unit being adjusted turns ratios on the HV transformers. Each HVPS provides its TWT's nameplate voltages and/or currents within the accuracies shown in Table 3.2.3-1 when the TWT requirements are within the range shown in Table 3.2.3-2. Figure 3.2.3-4 shows how these specifications relate to the current and power requirements of each of the individual high voltage modules (cathode and collectors).

Table 3.2.3-1. HVPS Output Requirements

Output	Magnitude Accuracy Including Regulation (Steady State)		
	TWT in Conduction		TWT Cutoff
	TWT at Saturation	Without RF Drive	
Cathode Voltage (E_k)	$\pm 0.25\%$	$\pm 0.25\%$	$\pm 0.25\%$
Collector 4 Voltage (E_{b4})	$\pm 2\%$	+ 5%, - 2%	$\pm 10\%$
Collector 3 Voltage (E_{b3})	$\pm 2\%$	$\pm 5\%$	$\pm 10\%$
Collector 2 Voltage (E_{b2})	$\pm 2\%$	$\pm 5\%$	$\pm 10\%$
Grid to Cathode Voltage (E_{gk})	$\pm 1\%$	$\pm 1\%$	+ 20%, - 0%
Filament Current (I_F)	+ 0.5%, - 1.5%	+ 0.5%, - 1.5%	+ 0.5%, - 1.5%
Ion Pump Voltage	+ 20%, - 10%	+ 20%, - 10%	+ 20%, - 10%

The TWT requires two other dc inputs; cathode heater current and ion pump voltage. The interface requirements for these two inputs are also shown in Tables 3.2.3-1 and 3.2.3-2.

Table 3.2.3-2. TWT Power Requirements Ranges

Electrode	Voltage****	Current at Saturation	Current With No RF Drive	Current at Cut-Off
Cathode (E_k)	-8.00 ± 0.50 KV	58 ± 7.5 ma	58 ± 7.5 ma	0.1 ma maximum
Collector 4 (E_{b4})	-6.10 ± 0.50 KV	20 ± 15 ma	57 ± 7.5 ma	0.1 ma maximum
Collector 3 (E_{b3})	-3.70 ± 0.50 KV	20 ± 15 ma	5.5 ± 5.0 ma	0.1 ma maximum
Collector 2 (E_{b2})	-2.90 ± 0.50 KV -0.70 KV	25 ± 12 ma	5.5 ± 5.0 ma	0.1 ma maximum
Body	0 V	6 ± 3 ma	3.0 ± 2.5 ma	0.1 ma maximum
Grid During Conduction	$+300 \pm 150^*$	500 μ A maximum	500 μ A maximum	---
Grid at Cut-Off	-500 V*	---	---	100 μ A maximum
Cathode-Heater	-3.2 ± 0.5 V*	1.5 ± 0.3 ADC	1.5 ± 0.3 ADC	1.5 ± 0.3 ADC
Ion Pump	$+3.0$ KV	5 μ A maximum**	5 μ A maximum**	5 μ A maximum**

* Voltage with respect to cathode; all other voltages with respect to body.

** Turn on transients of up to 100 μ A will be permitted and the ion pump voltage will not drop below +2.7 KV.

*** Maximum power required by the TWT is assumed to be less than 265 Watts during conduction.

**** Additional restrictions on cathode and collector voltages.

$$|E_k| > |E_{b4}| > |E_{b3}| > |E_{b2}|; 2.9 \text{ KV} \geq |E_k - E_{b4}| \geq 1.3 \text{ KV}; 2.9 \text{ KV} \geq |E_{b4} - E_{b3}| \geq 1.7 \text{ KV};$$

$$1.5 \text{ KV} \geq |E_{b3} - E_{b2}| \geq 0.3 \text{ KV}$$

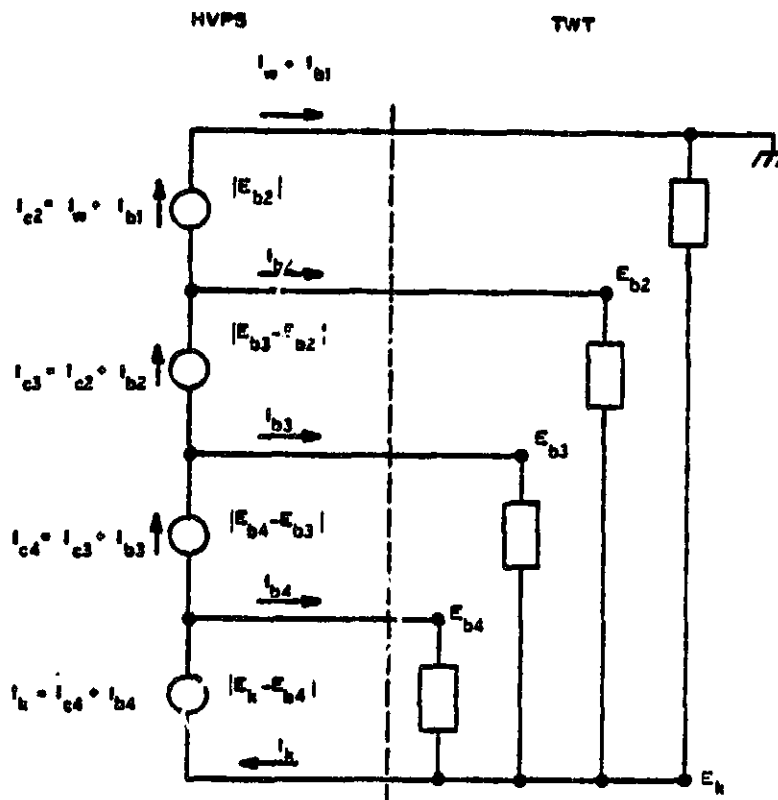


Figure 3.2.3-4. TWT Power Flow Diagram

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Although many of the elements of the HVPS will not be described herein, a complete block diagram is presented in Figure 3.2.3-5 to provide the reader with a general overview of the basic functional requirements.

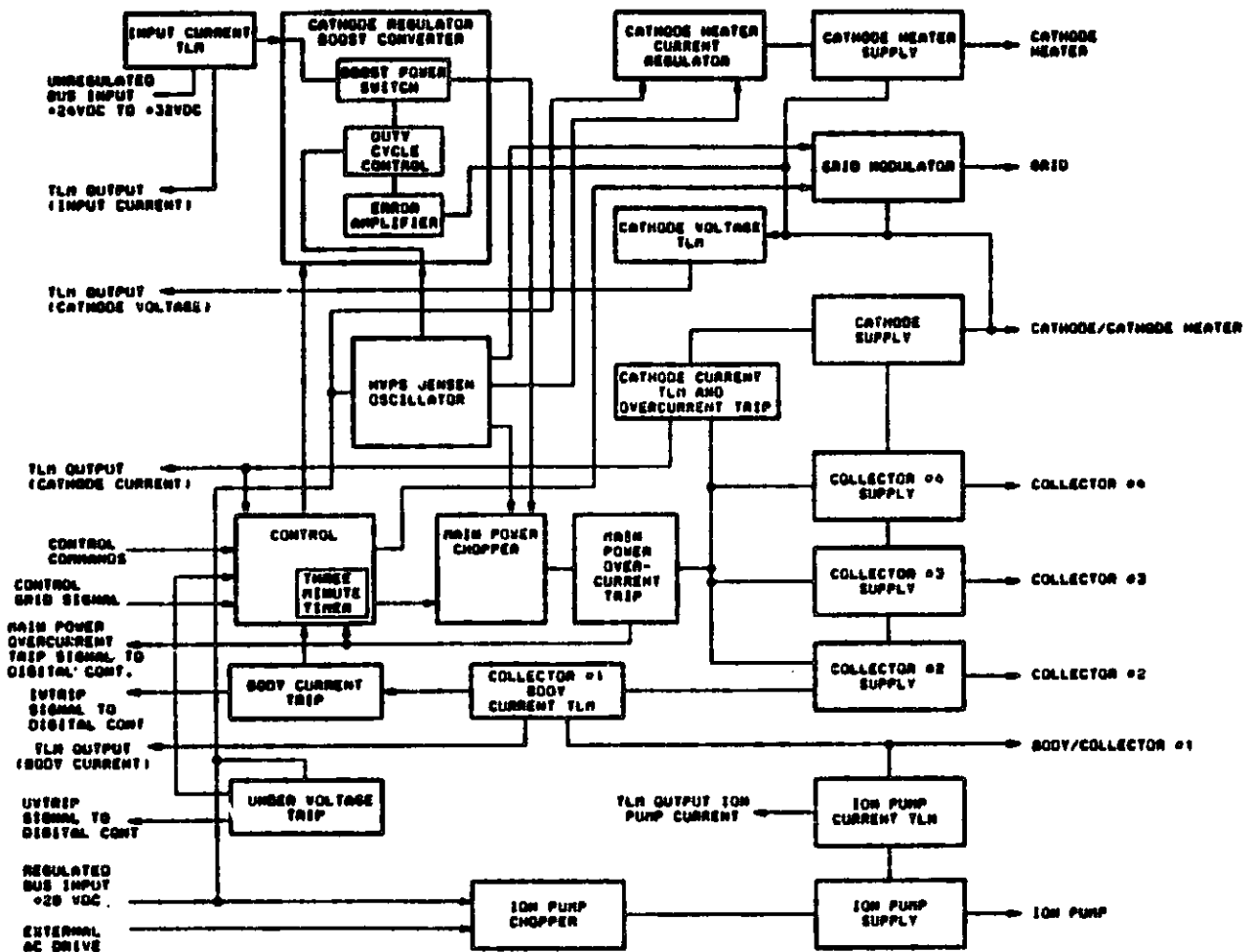


Figure 3.2.3-5. Block Diagram - NROSS HVPS

Cathode Voltage Regulation Loop. Due to the magnitude and pulsed nature of the power required by the cathode and collector supplies, power for these supplies was drawn directly off the spacecraft unregulated bus (battery bus) for the SASS Scattometer. This was necessary to help minimize EMI generated by the pulse

current and to provide sufficiently low source impedance to achieve adequate transient performance. For NROSS the HVPS will receive power from a regulated power supply and we are told that the supply output droops 1.4 volts during the 5 ms 15 amp (max) current pulse. This droop will adversely affect the transient performance of the HVPS so that the rise time (time from XMIT command until voltages have stabilized so that RF signal can be applied) will increase from 1.0 ms for SASS to 1.5 ms for NROSS. This extra delay can be accommodated but it has the effect of lengthening the XMIT/REC cycle by 0.5 ms which reduces the max. number of XMIT/REC cycles per antenna dwell period from 39 to 38. The resulting degradation of instrument performance is small; but, there may be other reasons for not operating at the wax pulse rep rate (such as Scatt Processor logic speed limitations or synchronization of the Scatt to spacecraft data system rates) so the limitations imposed by the HVPS may become a mute point. The fall time of the power pulse may also increase slightly from the 0.2 ms required for the SASS instrument. The effect of using a regulated supply (instead of Battery Bus) on EMI must be investigated further and it must be pointed out that HVPS efficiency may degrade but the amount of degradation is hard to calculate since reduced efficiency due to the 1.4V sag is compensated for by increased efficiency due to operation close to 28V (instead of the full 24 to 32V range).

Since the unregulated bus voltage on SASS varied between 24 and 32 Vdc, a switching type ("non-dissipative") regulator was selected in order to maintain reasonable efficiency. As Figure 3.2.3-6 indicates, a boost type converter was selected for this application. Its average output voltage (voltage at Point D) is primarily a function of the conduction time of the boost transistors (duty cycle), the turns ratio of the autotransformer and the input voltage.

An autotransformer was selected for this application since it maximizes efficiency while minimizing weight to accomplish this function. With this approach, the boost converter switches only the amount of power necessary to raise the output voltage to the required value above the input voltage. In closed loop operation, t_{on} is adjusted to maintain the cathode voltage (E_K) at its appropriate value. The boost output voltage (50V) is applied to the center taps of the cathode and collector module HV transformers (T2 through T5). Chopper transistors Q3 and Q4 switch the HV transformer primaries in parallel, and all draw their power through a common inductor.

The module outputs are stacked in series to generate each collector voltage and finally the cathode voltage. Since each module has to develop only the incremental voltage between two adjacent electrodes the piece part voltage requirements are minimized. As a result the modules are smaller and more reliable; the transformers are easier to build and impregnate; and the piece part selection is greater. The modular approach simplifies the top assembly design and makes the unit easier to build and repair. All of the modules are of similar design with the major difference being the turns ratio of the individual

transformers. Each module contains a voltage step up transformer, a capacitive voltage multiplier, an output current limiting resistor and a preload (bleeder) resistor. The use of the capacitive voltage multiplier reduces the transformer secondary turns by a factor of two. This makes the transformer smaller and lowers the secondary interwinding capacitance. The output current limiting resistors limit the peak current during arcing thus controlling the stresses on both the tube and the HVPS output filters. In addition, the current limiting prevents excessive voltage transients on the output power return line during arcing. Collector voltage regulation effects due to filter peak charging during the "no load" portion of the cycle are reduced by providing a bleeder load across each module output.

Electrostatic shields are used to minimize the effects of interwinding capacitance from primary to secondary and to minimize voltage stress concentrations. A porous polyester fibermat tape insulation material is used to provide physical spacing and to allow complete impregnation of the windings. The tape has good electrical properties when impregnated. The module is encapsulated in a one-step potting process.

The cathode voltage is sensed and fed back to the error amplifier where it is compared to a reference voltage. The error amplifier output signal is used to adjust the boost duty cycle via the compensation amplifier and the duty cycle controller. The compensation amplifier transfer function provides the necessary compensation to guarantee loop stability and the duty cycle controller controls the conduction time (t_{on}) of the appropriate transistor (Q1 or Q2) in response to its analog input signal.

Since this system is required to operate from no load to full load, a demand drive scheme was used to provide base drive to transistors Q1 through Q4. The emitter current of each transistor is sensed via N3 of its drive transformer. The turns ratio (N2/N3) provides the base drive mechanism during the transistor conduction time to assure a forced drive ratio of ten while the "primary" winding of the drive transformer (N1) provides a means for "gating" the transistor on and off. This highly efficient drive techniques ensures adequate drive while

maintaining acceptable transistor switching characteristics as a function of load. In particular this method minimizes variations in transistor storage time versus collector current, assures high speed switching and guarantees low saturation (V_{CESAT}) voltages even during transient conditions.

Table 3.2.3-3 presents actual measured static performance data for this system. Comparison of the measured data and the requirements shown in Table 3.2.3-1 shows that all results are well within specifications when a "stiff" battery input bus is used. The full load condition (TWT @ RF saturation) efficiency for this system is approximately 85%.

Table 3.2.3-3. Cathode and Collector Supplies Regulation Data

Parameter	Nominal Value	Measured Value/% Deviation From Nominal		
		TWT at RF Saturation	TWT Grid Biased ON No RF Drive	TWT Grid Biased to Cut-off
E_K	-8.10 KV	-8102/+0.025	-8101/+0.021	-8103/+0.037
E_{b4}	-6.200 KV	-6180/-0.32	-6212/+0.19	-6122/-1.26
E_{b3}	-3.800 KV	-3795/-0.13	-3780/-0.53	-3688/-2.95
E_{b2}	-3.200 KV	-3193/-0.22	-3178/-0.69	-3117/-2.59

Grid Modulator. The grid modulator is the most unique circuit in the HVPS. It is required to switch the grid voltage between approximately +300V and -500V with respect to the cathode voltage. Further, the conduction voltage (+300V) must be regulated to within one percent and the rise and/or fall time of the switching waveform must be less than 200 microseconds as indicated by Figure 3.2.3-7. A block diagram of the grid modulator is provided in Figure 3.2.3-8.

The grid converter provides two high voltage outputs of opposite polarity stacked in series, and a low voltage bias supply for the grid regulator electronics. Since both the cut-off and the conduction voltages are with respect to the cathode potential, the grid converter transformer and the HV switch control

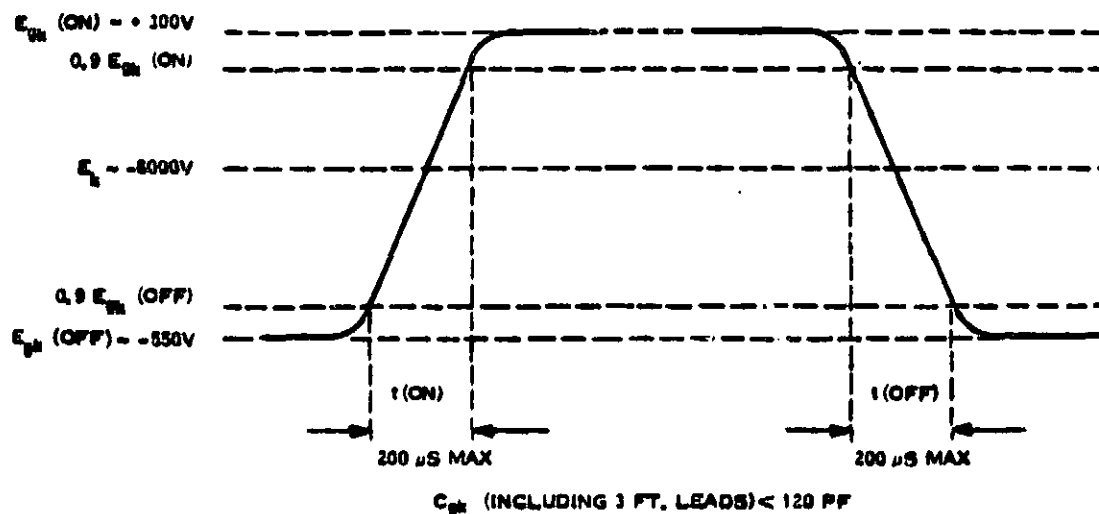


Figure 3.2.3-7. Grid Modulator Switching Speed Requirements

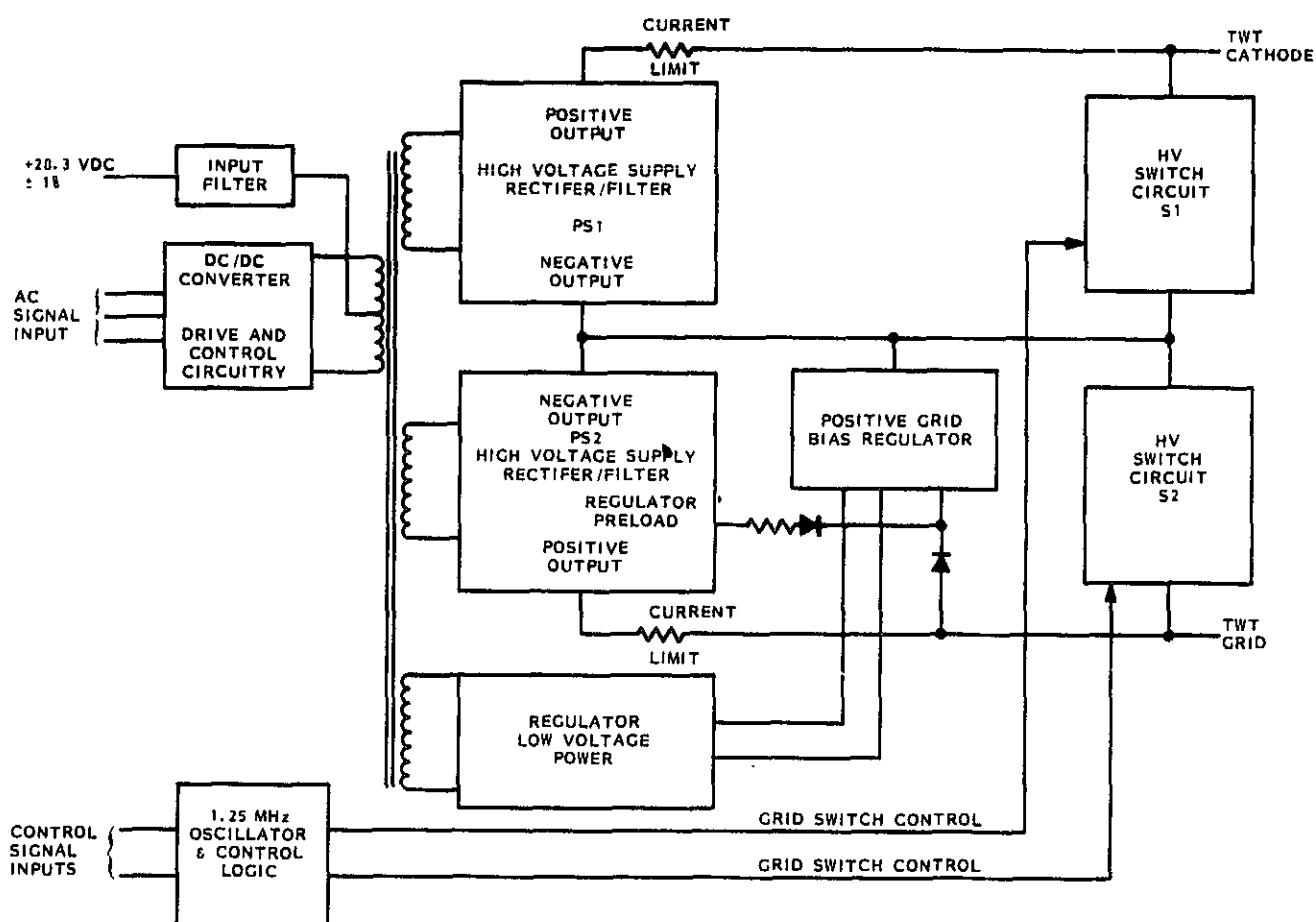


Figure 3.2.3-8. Grid Modulator Block Diagram

isolation transformers must be designed to stand off in excess of -8KV. With HV switch S1 turned on and S2 turned off, PS1 is shorted out and PS2 is connected between grid and cathode thus biasing the grid to the conduction potential. With S1 switched off and S2 on, PS2 is shorted and PS1 is connected between grid and cathode and the TWT is biased to cutoff.

High frequency high voltage isolation signal transformers are used to couple the HV switch control signals from ground potential to the cathode potential. The control logic ensures that the appropriate switch status is maintained and that one switch is always on and the other is off. The grid is biased to cut-off during both the cathode voltage turn on and off transients even during fault conditions. This precaution has been taken to eliminate potential damage to the TWT caused by high body current transients. With the cathode voltage between approximately $0.1 E_K$ and $0.9 E_K$, the electron beam is not focused and most of the current is intercepted by the TWT body. Also, when the grid is being switched the same kind of defocusing occurs. By biasing the grid to cut-off during the E_K turn-on and turn-off transients and by insuring high speed grid switching, the potential thermal damage associated with high body current transients during normal operation is eliminated.

Tables 3.2.3-4, 3.2.3-5 and 3.2.3-6 present regulation, switching speed and input power performance characteristics for a prototype grid modulator. Note that all measured values are well within specification.

Table 3.2.3-4. Grid Modulator Regulation Performance

Maximum deviation from nominal output voltage vs. temperature.

Line Change - $\pm 2\%$

Load Change - + 300 V output -- 0 to 500 μa
 - 550 V output -- 0 to 100 μa

	Temperature			Spec
	-10°C	25°C	+ 85°C	
+ 300 Volt Output	+ 0.14%	- 0.08%	-0.22%	$\pm 1\%$
- 500 Volt Output	- 3.51%	- 1.04%	+ 5.95%	$\pm 10\%$

Table 3.2.3-5. Grid Modulator Switching Performance

$V_{in} = 28.3 \text{ V}$		$T_A = 25^\circ\text{C}$	
Grid Bias Mode		Pin	
Conduction		3.82 Watts	
Cut-off		2.83 Watts	
Pulsing (20% Duty Cycle)		3.11 Watts	

Table 3.2.3-6. Grid Modulator Input Power Characteristics

$C_{gk} = 150 \text{ pf}$				
	Temperature			Spec
	-10°C	$+25^\circ\text{C}$	$+85^\circ\text{C}$	
Turn On	80 μs	55 μs	72 μs	200 μs
Turn Off	100 μs	95 μs	116 μs	200 μs

TWT/HVPS Protection Characteristics. Very briefly the HVPS provides several features designed to protect both the TWT and the HVPS both during ground testing and during normal on orbit operation. These protection features are as enumerated below.

1. Load Current Limiting. Load currents resulting from momentary load shorts (arcs) do not exceed 100 amps peak - (spec 1000 amps max).
2. Ion Pump Voltage Application. Ion pump voltage is applied to the TWT prior to the application of cathode - heater voltage or cathode voltage and is present whenever these voltages are applied.
3. Stored Energy. The total stored energy available at any TWT electrode is less than 0.8 joules - (spec 45 joules max).
4. Warm-up. Cathode - heater voltage is applied to the TWT for 180 ± 20 seconds prior to the application of cathode voltage.
5. Cathode Heater Current Transients. The filament current does not exceed $1.2 \times I_f$ amperes under any load or transient condition.

6. Body Current Trip. The cathode and collector voltages will be removed from the TWT if the body current exceeds 10 ± 1 maDC and further the trip will occur within 5 ± 1 ms for a body current step of 0 - 18 ma.
7. Cathode Voltage Turn-On. The cathode and collector voltage will be applied with the grid biased to cut-off.

3.2.3.2.2 Design Status

The mechanical and electrical designs of the HVPS is identical to that of the Seasat A Satellite Scatterometer except for a small modification required for the filament regulator.

3.2.3.2.3 High Voltage Power Supply Packaging

The HVPS proposed is the identical design used on Seasat, and the ROM Cost Proposal does not include any design modification for NROSS. This power supply was designed for a one (1) year mission life and operated flawlessly for the abbreviated Seasat mission. The long life characteristics of this design is not known, but is estimated to be better than any of the three BSE HVPSs which operated in space between 28 months and 30 months.

3.2.3.3 TWT Power Monitor

Following the TWT is a directional detector which is used to monitor the TWT RF output power for health check and calibration purposes. The component is essentially a waveguide directional coupler with an integrated detector diode set and DC conditioning circuitry all combined into one assembly. The design to be used is identical to that employed with the 100 Watt TWT on the Seasat A Scatterometer Program and has proven to be stable and accurate to within ± 0.5 dB at full output power over its full operating temperature range.

3.2.3.4 Antenna Switching Matrix (ASM)

The ASM will route microwave signals between the transmitter/receiver and antennas for the NROSS Scatterometer. It is inserted between the six antennas, and the remaining portions of the Scatterometer radar system and routes the RF transmit power from the TWT to the selected antenna. The ASM also decouples the transmitter from the receiver and routes the backscattered energy from the same antenna to a low noise receiver. A means for injecting a noise signal for receiver calibration is also provided by the ASM.

The most cost effective approach is to use the ASM already designed for the SASS program even though this design has 8 antenna ports compared to the 6 required for NROSS. In the SASS design circulators 1 thru 4 (see Figure 3.2.3-9) controlled polarization selection and were all switched together by one control signal; circulators 5 and 6 controlled fore/aft selection and switched together by one control signal. Circulator 7 (Left/Right selection) and circulator 8 (XMIT/REC) each had their own control signals.

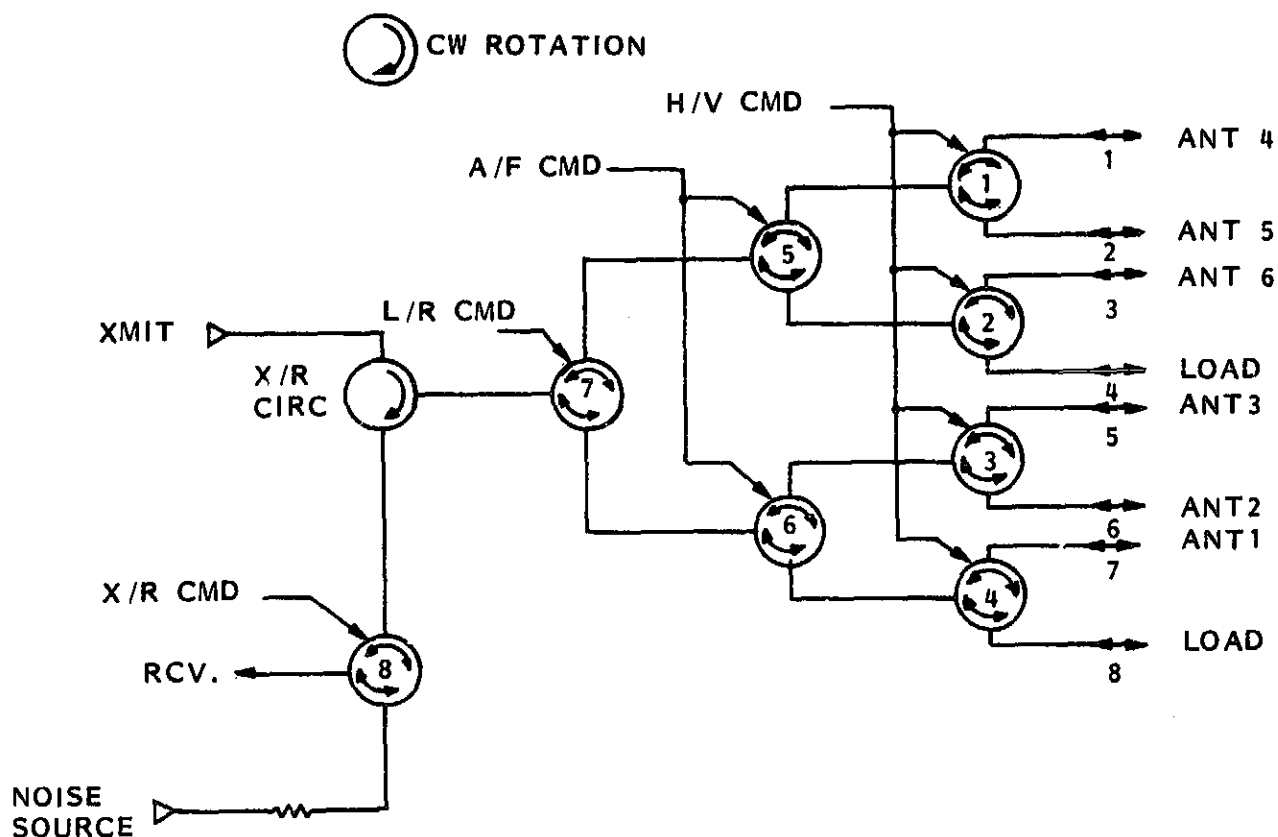
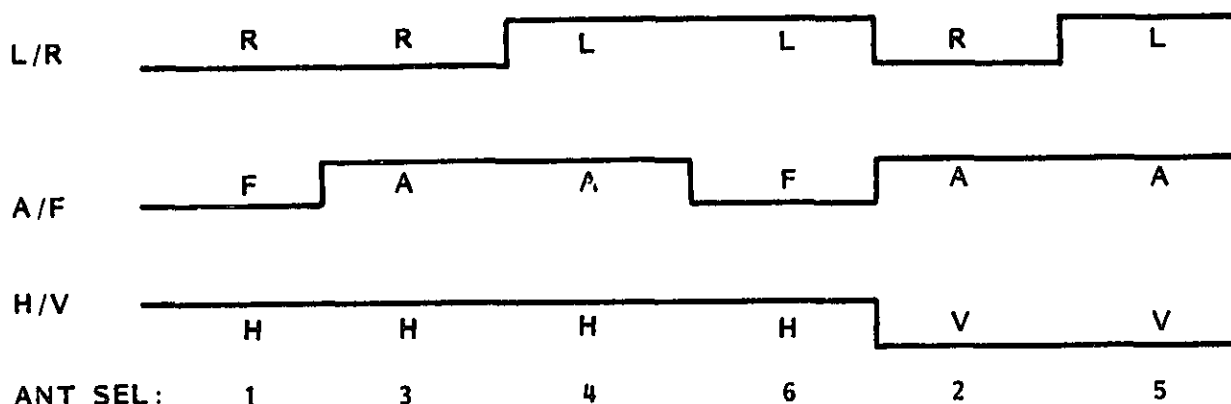


Figure 3.2.3-9. Antenna Switching Matrix Assembly

By terminating ports 4 and 8 of the SASS ASM with high power loads and a command sequence as shown in Figure 3.2.3-10 the antenna sequence required by the NROSS Spec can be implemented. Other sequences are possible by different command sequences.

**CIRC CMDS
(SASS NOMENCLATURE)**



COMMANDS SHOWN FOR XMIT (OPPOSITE FOR RECEIVE) AND
ANTENNAS CONNECTED TO ASM PORTS PER FIG. 3.2.3-9

Figure 3.2.3-10. Command Sequence for 1,3,4,6,2,5 Antenna Select Sequence

As shown in Figure 3.2.3-9, the assembly contains eight latching ferrite junctions, seven of which serve to select the desired antenna. The eighth latching ferrite junction is for added receiver protection during transmit pulses and provides an attenuated path which permits the injection of a calibrated noise level into the receiver. The assembly also contains a transmit/receive ferrite junction for decoupling.

3.2.3.5 Waveguide and Coax Components

The transmitter waveguide and coax components will be used to interconnect the various circuit elements of the NROSS Scatterometer Transmitter. Included in the components are the Waveguide Component #1, Waveguide Component #2, the TWT Input and output isolators, and the Low Pass Filter.

Most of the waveguides designed for SASS are directly applicable for the NROSS Scatterometer. Each assembly will be made from dip-brazed aluminum pieces and will incorporate sections of flexible waveguide to absorb vibration and motion. The filters used for SASS were designed using proven computer programs. Since the transmit frequency for the NROSS Scatterometer is slightly different, it may be necessary to modify the iris dimensions using the computer program to compute the design values. All waveguide components will be thoroughly tested and characterized using the automatic network analyzer.

3.2.4 RECEIVER

3.2.4.1 Overall Description

The Scatterometer Receiver will receive the doppler-shifted return signals via the antenna, establish the system noise temperature, provide amplification and downconversion of the received signal, and output the signal to the Integrated Electronics Assembly (IEA). A broadband noise source will be used to calibrate the gain of all measurement channels of the receiver and processor.

Referring to Figure 3.2.4-1 the backscattered return signals (or internal calibrate signals) at 13.995 GHz are directed through the circulators of Antenna Switching Matrix (ASM) to the RF amplifier which is a GaAs FET Low Noise Amplifier (LNA) exhibiting 30 dB of gain and having a maximum noise figure of 4.5 dB. Total system noise temperature achievable with this design should not exceed 1365°K, including front end losses and a 200°K antenna temperature. The output of the LNA is filtered to limit out-of-band interference and images, and then applied to the downconverter mixer where it is combined with the 14.192 GHz signal provided by Waveguide Component #1 of the transmitter section. The gain of the receiver from the input of the ASM to the input of the IEA is nominally 50 dB. The 197.112 MHz IF input signal to the IEA is then amplified and filtered to limit noise and mixed once again in the 2nd IF, with signal from the switched local oscillator. If the system is working from a forward-looking antenna, then the doppler shift expected is positive with respect to the carrier. In this case the switched local oscillator will be commanded to produce a 188.899 MHz output and the second IF will be at 8.213 MHz with the doppler spread spectrum running above this frequency. To eliminate the need for a negative doppler processing channel, all that is needed is to shift the switched local oscillator to 205.325 MHz when the expected returns are of negative doppler characteristics. In this case the mixing in the 2nd IF inverts all signals (e.g., $197.112 - f_{DOP} - 205.325 = -(8.213 + f_{DOP})$) and also produces a second IF with positively distributed shifted returns. Thus, all I-Q processing can be done at one IF frequency and with one set of low-pass filters. Following the second conversion mixer there is an additional noise limiting filter, amplifier, four-way power divider, and finally the individual quadrature (I-Q) mixers and Low Pass Filters

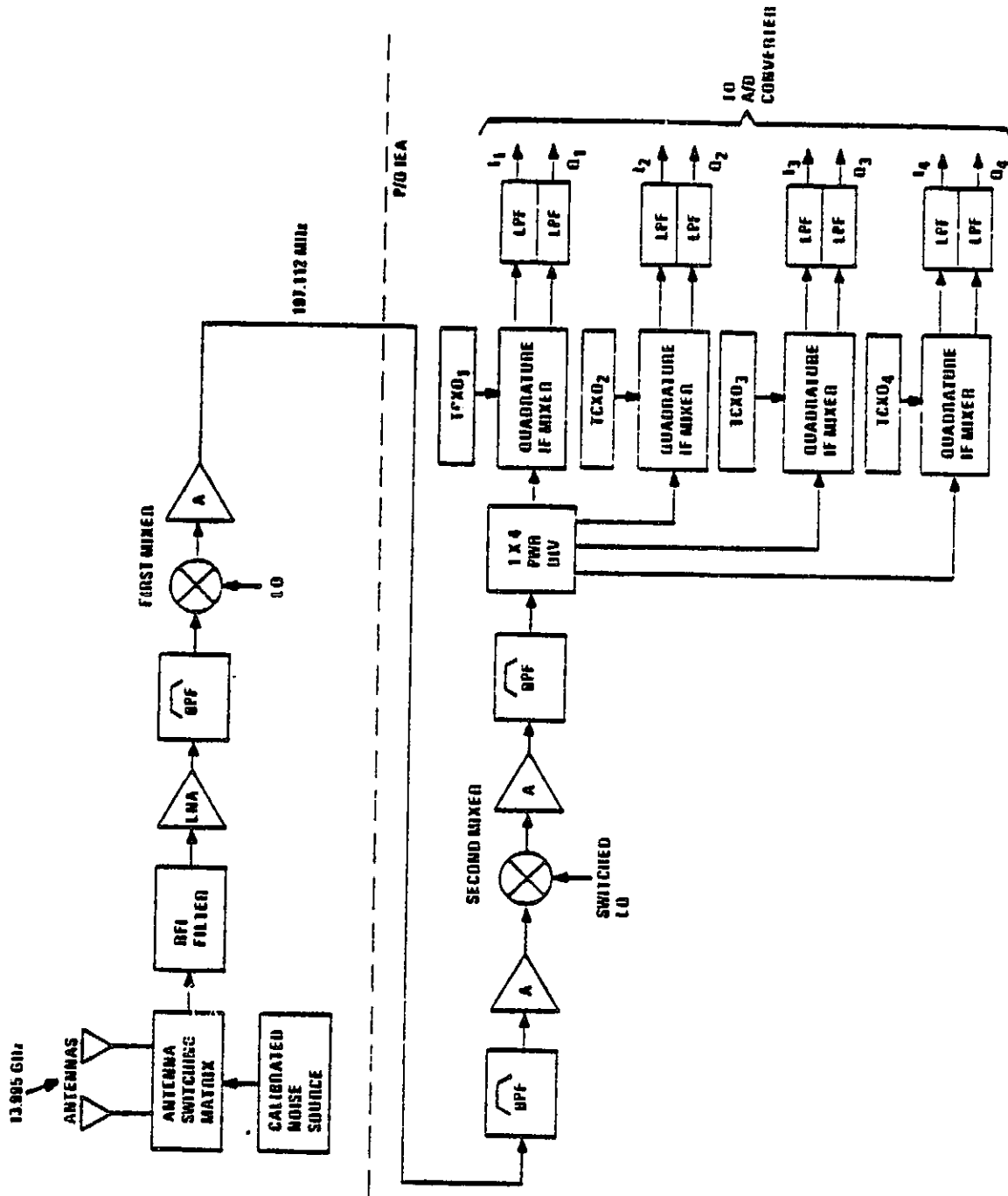


Figure 3.2.4-1. Scatterometer Receiver Functional Diagram

(LPF's) associated with each processing channel. These last sections, from the second conversion through the LPF's will be integrated with the Scatterometer Processor into the Integrated Electronics Assembly.

3.2.4.2 Low Noise Amplifier (LNA)

The Low Noise Amplifier will provide low noise amplification of the Ku-Band, doppler-shifted return signals. Because of the low signal levels and noiselike characteristics of the return signals, the LNA characteristics of high gain, low noise figure, gain stability, spectral performance and linearity are of primary importance.

The LNA planned for the Scatterometer is a five balanced stage amplifier built with GaAs/FET chips. The FET approach was selected in preference to a tunnel diode because of its higher overload signal handling capability, greater dynamic range and lower noise figure characteristic. The preferred GaAs/FET chip is the NEC V388 since it has been space qualified. The NEC V137 FET has a lower noise figure capability but as yet is not space qualified. In the event that the V137 is qualified in time for application to the Scatterometer LNA, it will be further considered.

Standard MIC technology is available for fabrication of the amplifier. The FETS are mounted on a Kovar carrier and bond wires connect the FET elements to strip transmission line circuits built on alumina substrates adjacent to the FET. Chip capacitors and resistors are epoxy attached to the substrate. Circuit matching turning elements are formed by transmission lines whose lengths are adjusted by bond wires between the lines and adjacent tuning pads.

Gain compensation with temperature is achieved by controlling a PIN diode attenuator between the third and fourth, or fourth and fifth, stages of the amplifier. The control signal for the attenuator is derived from a bridge network whose arms include temperature sensors located in the vicinity of the amplifier FETS.

An internal voltage regulator furnishes prime power to the RF circuits. To reduce size and weight, the regulator and its support electronics are also built on a substrate.

3.2.4.3 Calibration Assembly

The Calibration Assembly will provide a Ku-Band broadband noise signal over a sufficient bandwidth to calibrate the gain of all measurement channels in the Scatterometer Processor.

The Calibration Assembly consists of a solid state Ku-Band noise source, a dc current source, an isolator and waveguide to coax adaptor as shown in Figure 3.2.4-2. The design, except for operating frequency, is the same as used on SASS. The solid state noise source will be purchased from Microwave Semiconductor Corp. and shall have the performance characteristics as listed in Table 3.2.4-1. When in the calibration mode, the resulting receiver system Excess Noise Ratio (ENR) is approximately 20 dB due to the 10 dB attenuator which is located in the ASM and in the receiver calibration noise path.

An isolator is employed at the output of the noise source which provides a broadband match load for the solid state microwave source and also provides isolation to any transmitted power level that may be at the ASM-Calibration Assembly interface.

3.2.4.4 RFI Filter

The RFI filter will be a high-performance quasi-elliptic design located between the Antenna Switching Matrix and the receiver that provides 80 dB rejection of the altimeter radar chirp spectrum (13.56 ± 0.16 GHz) with minimal attenuation of the Scatterometer signal. This filter has a six pole response with a single transmission null on each side as shown in Figure 3.2.4-3. It will be realized in three cylindrical dual-mode, TE_{111} cavities, each of which contains two tuning screws plus a coupling screw. The internal cavity dimensions are approximately 0.737 inches in diameter by 0.540 inches long. The input and output waveguide ports will be located at opposite ends and rotated by 90 degrees with respect to one another. Careful design of the coupling apertures and tuning screw penetrations will yield an unloaded Q greater than 4700 and hence an insertion loss less than 0.45 dB as shown in Figure 3.2.4-4.

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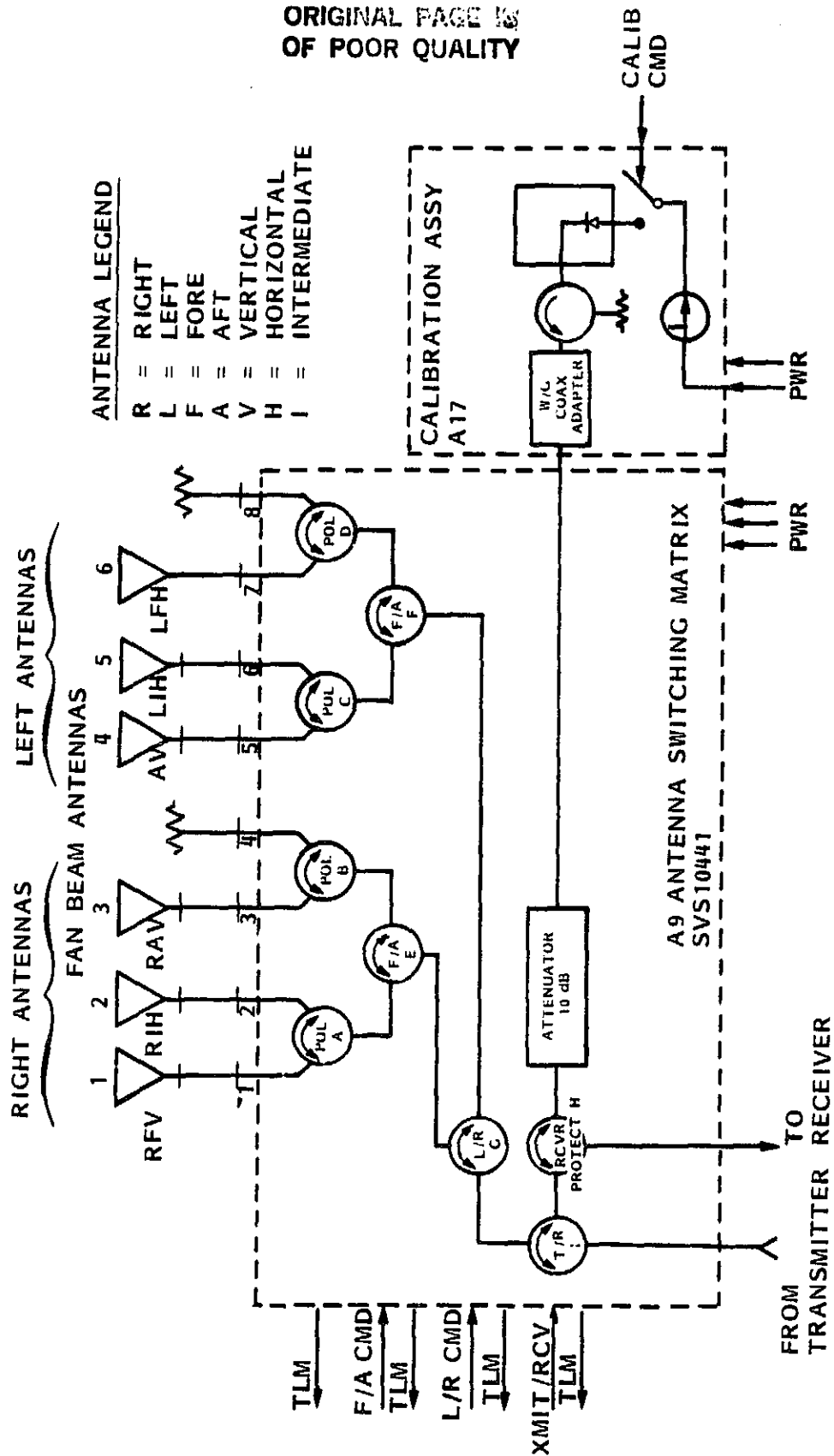


Figure 3.2.4-2. Calibration Assembly and ASM Interface

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Table 3.2.4-1. Noise Source Performance Characteristics
(Unless Otherwise Noted $T_A = 25^\circ\text{C}$)

Excess Noise Ratio (ENR)	29 dB min., 31 dB max.
Voltage Sensitivity	0.10 dB/% max.
Current Sensitivity	0.03 dB/% max.
Temperature Sensitivity (-10°C to $+55^\circ\text{C}$)	
Switching Speed	1.0 microsec. max.
Operating Speed	17.1 V min., 18.9 V max.
Operating Frequency (Minimum Range)	13.990 GHz min., 14.000 GHz max.
Incident RF Power	250 milliwatts max.

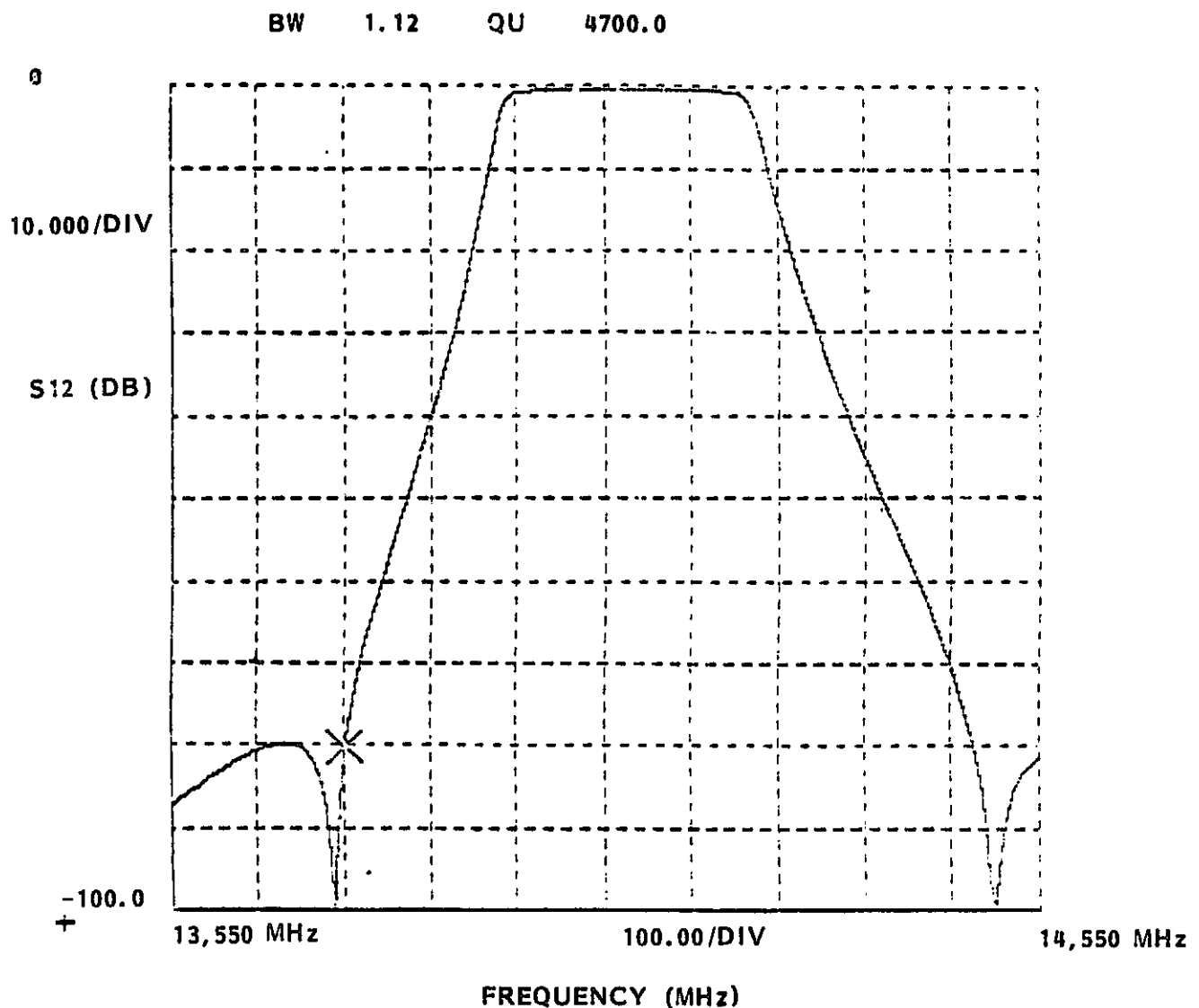


Figure 3.2.4-3. RFI Filter Response (Wideband)

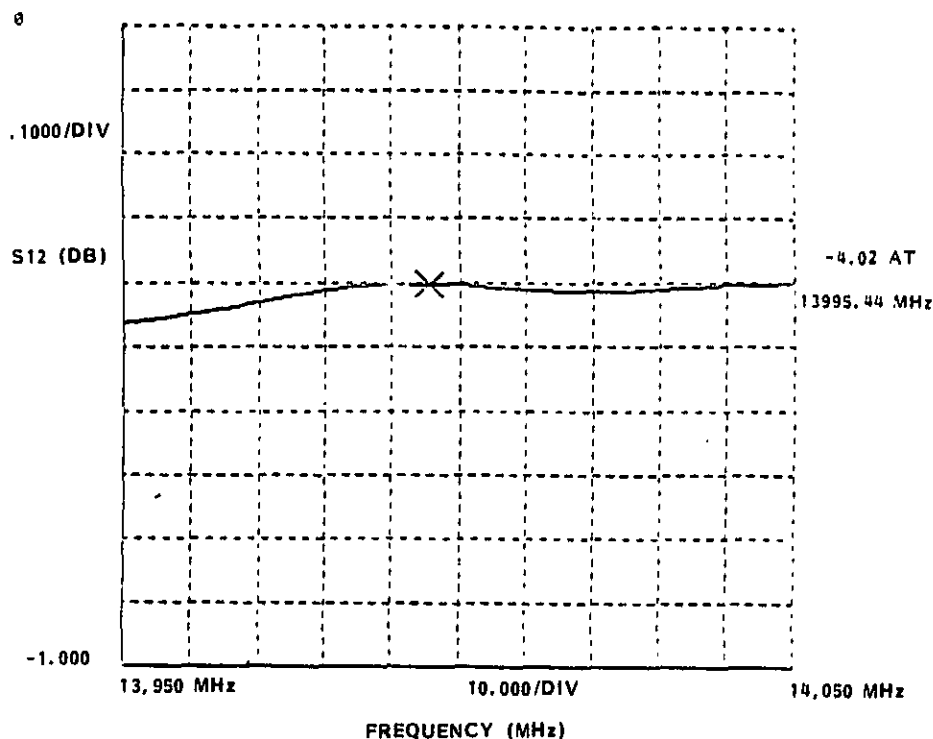


Figure 3.2.4-4. RFI Filter Response (Wideband)

A breadboard unit will be fabricated in copper to facilitate fine adjustment of the coupling apertures and cavity lengths. The EM and flight filters will be fabricated in silver-plated, thin-walled invar with laser welded joints near the center of each cavity to achieve low losses, good thermal stability and low weight. An automatic network analyzer and computer-aided alignment procedure will be used during the development and testing of these filters to ensure actual performance that is close to the theoretical.

3.2.4.5 First Mixer/Preamplifier

The first mixer/preamplifier will provide frequency conversion of the Ku-Band, doppler shifted return signals to an intermediate frequency of approximately 197.1 MHz and also provide low noise amplification of the IF signal.

The mixer/preamplifier will be the same design as used for SASS except for the slight difference in frequency of operation. It uses a MIC balanced mixer with about 8 dB conversion loss and feeds a 197.1 MHz FI amplifier that has a typical

gain of 30 dB. The mixer receives its local oscillator signal from the filtered output of waveguide Component #1 of the transmitter section. The LO level of 4.5 dBm provides optimum conversion loss. The gain of the IF preamp will be controlled to provide a stable gain across the operating frequency band.

3.2.4.6 Waveguide and Coax Components

The receiver waveguide and coax components will be used to interconnect the various circuit elements of the Scatterometer Receiver. Also included in the components are the Bandpass Filter (BPF) and isolator-adaptor used between the LNA output and the first mixer input.

Most of the waveguides designed for SASS are directly applicable for the NROSS Scatterometer. Each assembly will be made of dip-brazed aluminum pieces and incorporate sections of flexible waveguide to absorb the vibration and motion which may be encountered. The bandpass filter used for SASS was designed using proven computer programs. Since the receive frequency for the NROSS Scatterometer is slightly different it may be necessary to modify the iris dimensions using the computer program to compute the design values. All waveguide components are thoroughly tested and characterized using the automatic network analyzer. The isolator-adaptor provides isolation for the RF and LO ports of the first mixer and also provides a transition from WR62 waveguide to SMA coaxial connectors.

Since the RFI filter and LNA used for the NROSS Scatterometer are different designs than those used on SASS, it will be necessary to design some different waveguide components to interconnect these elements.

3.2.4.7 Flight Model Receiver

The flight receiver function is the same as described earlier in Paragraph 3.2.4 for the EM receiver except that the FM will be flight qualified.

Basic differences between the EM and FM receivers are:

1. The FM receiver will be fabricated with hi-rel flight parts.
2. The FM calibration assembly, LNA, and the first mixer components will be tested in thermal cycle, and random vibration environments whereas the EM components are only functionally tested.

3. The FM receiver will be exposed at the Scatterometer Subsystem level to the thermal vacuum, random vibration, acoustic, and EMC environmental testing whereas the EM receiver is only functionally tested in an ambient environment.

3.2.4.8 Receiver Spares

The receiver spares are the same as described earlier in Paragraph 3.2.4 except that the receiver spares will be exposed to acceptance level environmental tests. The only difference between the common environmental tests for the spares and the flight receiver is the level of the environments, with the flight receiver exposed to the greater limits.

3.2.5 INTEGRATED ELECTRONICS ASSEMBLY

The Integrated Electronics Assembly (IEA) contains the Scatterometer Processor, Digital Controller and a DC/DC converter which provides secondary voltages for the entire Scatterometer instrument, with the exception of most of the High Voltage Power Supply.

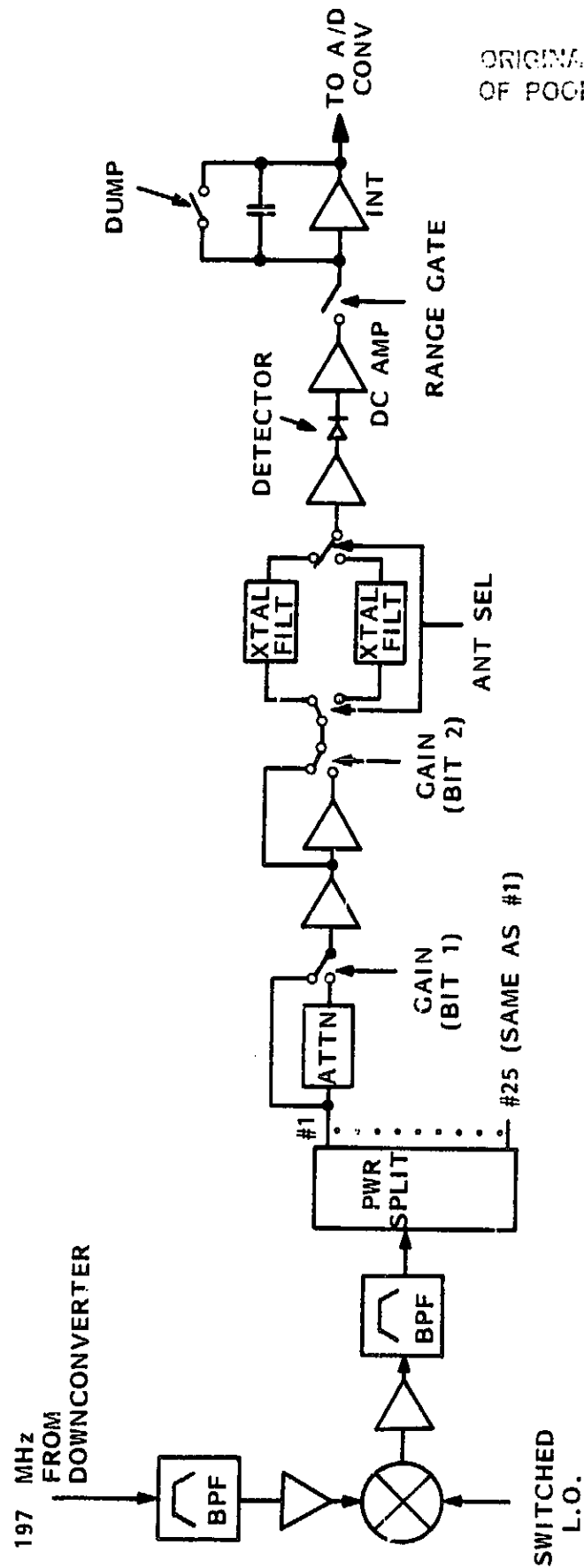
The Scatterometer Processor measures return power and outputs digital words corresponding to return power for each doppler cell. The Digital Controller receives commands from the Spacecraft, generates control signals to the Scatterometer instruments, accumulates and formats data and sends it to the Spacecraft.

3.2.5.1 Scatterometer Processor

3.2.5.1.1 Scatterometer Processor - Analog Version

An analog Scatterometer Processor with 25 Km Doppler cell size is described in this section for the NROSS mission. Note that the analog approach does not provide for on-board co-registration and therefore ground data processing is required to calculate the cross track distance of each Doppler cell as a function of antenna and orbit latitude. Also note that the ROM costing documented in Section 8.0 is for the Digital version - no costs were calculated for the analog version. A description of the Processor follows, refer to Figure 3.2.5-1 for clarification.

3.2.5.1.1.1 Second IF and Power Splitting. The 197 MHz 1st IF signal out of the Downconverter is bandpass filtered and amplified and then mixed with a switched LO signal to normalize the positive and negative doppler associated with forward and aft looking antennas. Note that antenna #5 should be changed from the configuration shown in the NROSS Spec (65° angle) to a 115° angle so that its doppler would be the negative of antenna #2 and so one set of filters could be used for antennas #2 and #5 by merely switching LO frequency. The output frequency of this second mixer will be about 8.2 MHz for all antennas since the positive and negative doppler has been normalized by using appropriate LO frequencies. Amplification and band pass filtering at 8.2 MHz follows the mixer. Up to this point, the analog and digital Scatterometer Processors are identical.



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Figure 3.2.5-1. Block Diagram, Analog Scatterometer Processor

The 8.2 MHz 2nd IF signals is then passed through a series of power splitters to obtain 25 signals and equal power which are inputs to the 25 doppler filter channels.

3.2.5.1.1.2 Gain Switching and Doppler Filtering. Because the dynamic range of the square law detector diode is less than the dynamic range of the signal, several discrete gain settings must be available before the detector. For SASS, 4 gain states were required, in 10 dB increments; for NROSS an analysis will be required to determine the dynamic range of the return for each doppler cell and the required number of gain steps must then be determined.

During each antenna dwell period, the gains are set to maximum for the first XMIT pulse. The amplitude of the first return pulse is compared against a threshold (this is done in the Digital Controller after A/D conversion of the integrator output) and if it exceeds the threshold the gain is lowered to the next level for the next transmit pulse. This is repeated two more times (if 4 gain states are used). Each of the 25 doppler channels goes thru this procedure during the first 3 XMIT/Rec cycles (for 4 gain states) and thus the data from these cycles cannot be accumulated and is lost. After the first 3 XMIT/Rec cycles the gain setting remains constant for each channel for the remainder of the antenna dwell period and the data can be accumulated.

The gain select circuitry is followed by a select switch which selects the doppler filters, 25 each, for either antennas 1, 3, 4, 6 or Ant 2 & 5. The filters for SASS were highly stable crystal filters; similar filters could be used for NROSS except they are fairly large and 50 filters would take up much space. SASS filters are much smaller and may be worth investigating. (This study was too limited to permit looking at SASS filters.)

The filter center frequencies and bandwidths would be chosen for some arbitrary latitude and for a compromise between left side and right side doppler and subsequent variations of the footprints cross track location as a function of latitude and antenna selected would have to be taken into account by ground software. The difference in doppler bandwidths of the $\pm 45^\circ$ antennas vs. the $\pm 65^\circ$ antennas necessitates two sets of filters, one for each set of antennas selected.

3.2.5.1.1.3 Detection, Range Gating and Integration. The signals from the doppler filters are buffered by an amplifier and a square law detector diode is used to derive a DC signal proportional to return power.

After a DC amplifier a "range gate" series switch is used to remove input from the integrator when the return pulse for the particular doppler cell is not present. This prevents integration of out of band signal and noise. The range gate timing takes into account the change in cell location as a function of latitude and antenna and hence is wider than the cell bandwidth at any given latitude; thus some out of band signal is integrated but the error introduced is small.

Opening the range gate switch also causes the integrator to act as a "Hold" circuit allowing one A/D converter to be time shared between 25 channels. After all channels are A/D converted a "DUMP" signal closes the switch around the integrating capacitor and resets the integrator. The integrators are dumped after every XMIT/Rec cycle and accumulations of return signal over an antenna dwell period is done digitally downstream from the A/D converter.

3.2.5.1.2 Scatterometer Processor - Digital Version

The Digital Scatterometer Processor considered for this study is basically the one proposed by GE for the NOSS program. In calculating the power and circuitry requirements the NROSS requirements were factored into the NOSS baseline (25 vs. 10 km cell size, 25 cells vs. 60 cells, etc.) as were any new and better circuit components which were not available for NOSS. However, the study was too limited in resources to permit re-examination of many key parameters, such as digital word length, windowing scheme, doppler frequencies, etc.

The following description of the Scatterometer Processor will elaborate on similarities or differences from the NOSS design; however, the major differences are as itemized below.

1. The larger cell size (25 km vs. 10 km) and the need for only one near Nadir cell reduces number of doppler cells from 60 to 25 for NROSS.
2. Availability of a faster 12 bit A/D converter reduces number of A/D and S/H circuits from 8 to 4.
3. Availability of larger memories and faster CMOS RAMS reduces power requirements for NROSS.
4. Availability of GE designed CMOS/SOS "Advanced Computational Element" CVLSI chip reduces part count and power for NROSS.
5. A problem discovered with the NOSS co-registration circuit increases chip count but power is minimally affected due to power strobing.

3.2.5.1.2.1 General Description. The Scatterometer is based on an FFT circuit to perform the gating and filtering function on the backscattered return signal. The individual outputs of the FFT are assembled into Doppler cells whose center frequency is adjusted as a function of antenna and orbit position to keep the cross track distance of each cell constant. Hann weighting is performed to increase filter selectivity.

The Scatterometer Processor block diagram is shown in Figure 3.2.5.1-1, its major functions are listed below.

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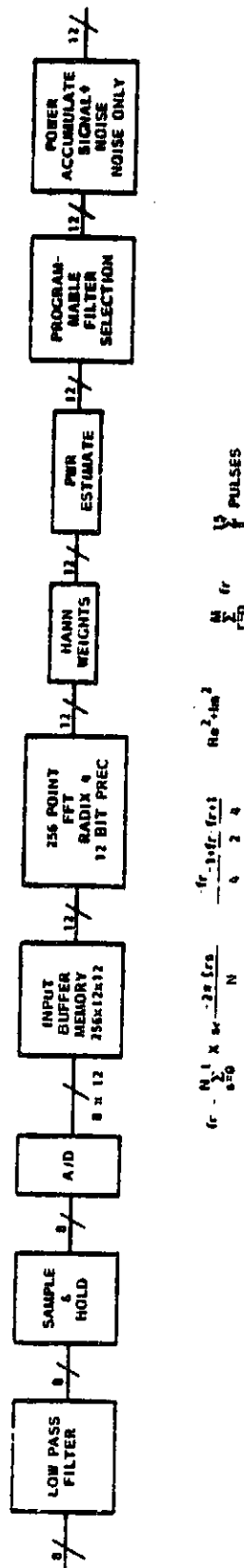


Figure 3.2.5.1-1. Processor Block Diagram

1. Sample and A/D convert four parallel complex signals representing the backscatter return signal in four separate but adjoining frequency bands.
2. Provide adequate input buffering such that the signal processing load can be averaged over the entire transmit period. A total of (8×256) 2048 complex words of 12 bits each will be processed each period.
3. Using the four complex input channels, four In Phase (I) and four Quadrature Phase (Q), perform eight Fast Fourier Transforms (FFT) of 256 points each period.
4. Hann weight the FFT outputs by convolving adjacent frequency bins in the appropriate manner.
5. Generate the power spectra by calculating $(RE_2 + IM_2)$ for each Fourier frequency bin.
6. Calculate the power spectra for 25 Doppler cells by accumulating the power of appropriate adjacent Fourier frequency bins.
7. Provide coregistration of the Doppler cells from beam to beam as a function of antenna and position in orbit.

3.2.5.1.2.2 Signal Processor Requirements Development. The ROM cost developed for this study includes the requirements development effort as described below.

The Signal Processor requirements are developed from the mission and instrument parameters. These parameters are the basis for the performance requirements of the digital signal processor. Two areas that define the processing requirements are pulse timing, and the time/doppler frequency characteristics of the return signal.

The pulse timing is a function of maximum and minimum round trip delays of the signal and hence of orbit altitude, swath coverage and spacecraft attitude. A first cut was taken at this timing during this study in order to scope the hardware, but a detailed analysis will need to be done during the development phase. It appears that transmit pulses occurring every approx. 16.5 ms will be required and since the antenna dwell time for an 830 km orbit and 25 km cell size is 627.3 ms, there will be 38 or 39 XMIT/Rec cycles per antenna per cell. (Two or three of these cycles should be Noise Only measurements, i.e., XMIT is inhibited.)

The time/doppler frequency characteristics of one representative beam are illustrated in Figure 3.2.5.1-2. The doppler frequencies result from the velocity of the spacecraft, rotation of the Earth, and the geometry of the transmitted and received signals. The function of the digital signal processor is to range gate and filter the backscatter energy from the ocean surface. The filter bandwidths correspond to 25 km cells on the ocean surface. The times and frequencies shown in Figure 3.2.5.1-2 are from a study done for the NOSS mission; they are only shown for reference to illustrate a typical case. The NROSS mission will have different frequencies and times, but the shape of the curves and the coverage of the return by 8 sets of FFT processes will be similar. This figure will vary as a function of antenna and orbit latitude, and one of the tasks for requirements development will be to calculate this figure for all antenna and orbit conditions and then to determine the bandwidths and timing of individual FFT's so that the entire return signal will be converted to 1024 discrete power spectral lines by the FFT processor.

3.2.5.1.2.3 Analysis Requirements. Analysis tasks necessary to finalize the detailed design requirements of the NROSS Scatterometer from the receiver IF Amplifier to the output buffer interface to the spacecraft telemetry must be included in the Scatterometer Signal Processor effort and have been included in the ROM cost estimate. These tasks can be divided into three fundamental groups.

1. Bandsplitting requirements.
2. Dynamic range requirements.
3. Coregistration requirements.

The bandsplitting requirements include definition of signal splitting phase and amplitude tolerances, specification of band definition filter requirements, and performance degradation predictions. In addition, the issue of cell and band definitions must be reviewed in conjunction with filter requirements in order to provide design/performance tradeoffs. Alternative bandsplitting and sampling designs should be investigated. The use of direct quadrature sampling of the second IF will be investigated to determine if it provides a more efficient use of resources (by eliminating the need for band shifting). This task will produce an alternate design to be compared with the present analog band splitting approach.

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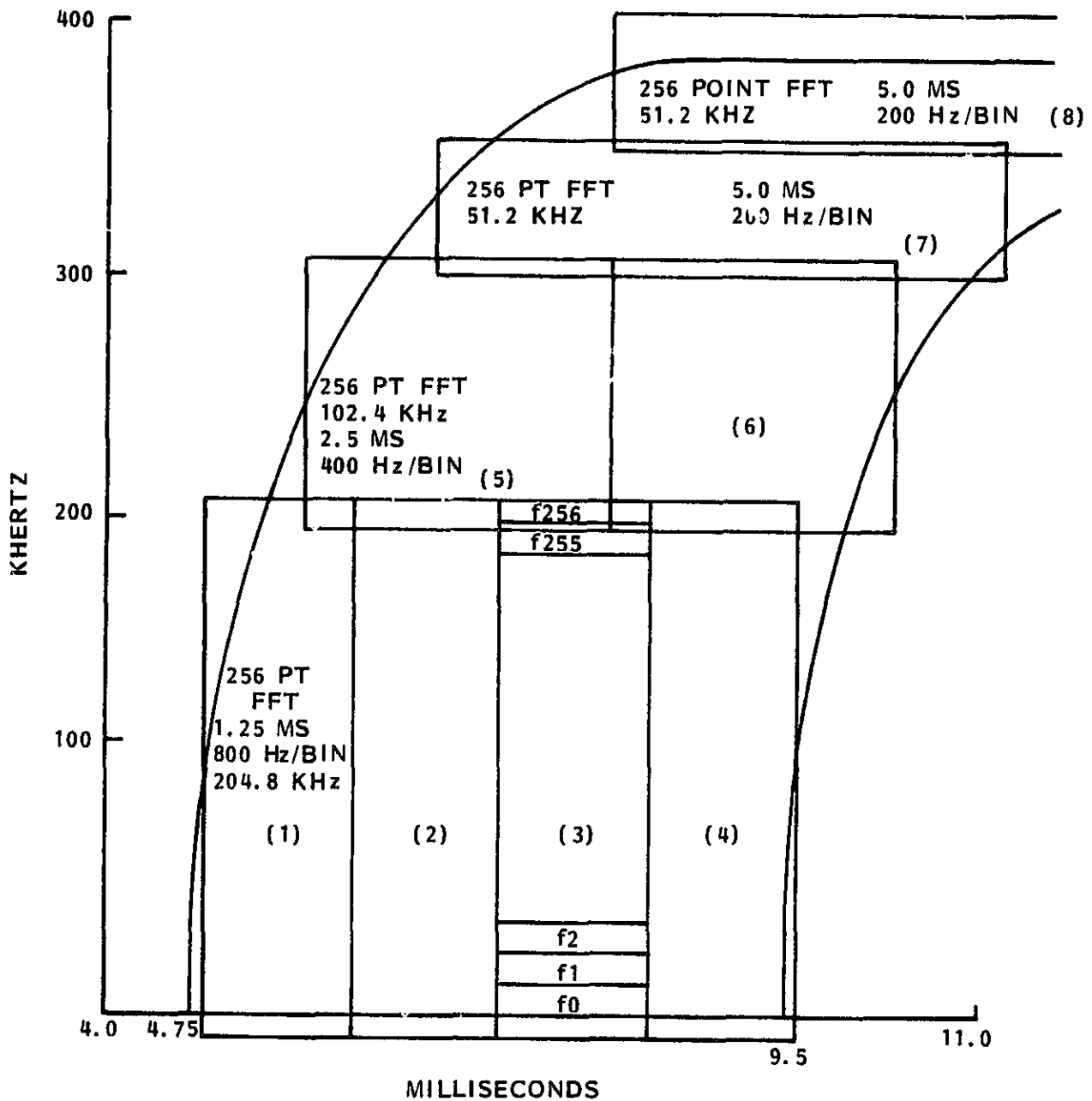


Figure 3.2.5.1-2. Return Signal

The issues of dynamic range and word length requirements will be studied with the intent of developing the most efficient hardware solution without sacraficing performance. The effects of finite quantization and saturation will be investigated along with errors generated with rounding and truncation. The results will be verified via simulation where appropriate.

The final study task addresses the problem of coregistration and the development of an algorithm for implementation. The Fourier filter bandwidths determine the ability of the processor to set the edges of the doppler cells. This question is also addressed in the setting of the band splitting requirements. The orbital requirements and the algorithms to define the adjustments to doppler center frequencies will be defined.

These study efforts should be completed in conjunction with the initial breadboard design phase of the Scatterometer Signal Processor. The results are to be verified in breadboard test and via simulation where appropriate.

Signal Processor Analysis and Design Support Tasks are listed below:

Task

1. Establish Signal Splitter Requirements to Define
 - a. Phase error effects.
 - b. Amplitude imbalance effects.
 - c. Combined effects.
 - d. Specification Requirements.
 - e. Numerical performance degradation of proposed design.
2. Establish Band Definition Filter Requirements to
 - a. Review cell requirements.
 - b. Review bin/cell synthesis.
 - c. Calculate cell-to-cell rejection.
 - d. Relate cell-to-cell rejection to system performance.
 - e. Define realistic filter requirements.

- f. Evaluate recommended filter's impact on system performance.
- g. Verify via simulation where appropriate.
- 3. Dynamic Range Requirements to
 - a. review existing requirements.
 - b. Calculate dynamic range expected in each band.
 - c. Establish word length requirement estimates.
 - d. Verify dynamic range compliance via simulation where appropriate.
- 4. Evaluate A/D Converter Requirements to
 - a. Establish a baseline A/D design in terms of word length and scaling.
 - b. Estimate performance degradation.
- 5. Analyze Bandsplit and Sample Alternatives to
 - a. Define alternate design(s); e.g., direct quadrature sampling.
 - b. Evaluate relative merits and requirements.
 - c. Recommend design approach.
- 6. Evaluate Coregistration and Orbit Update Requirements to
 - a. Define minimum spatial resolution requirements.
 - b. Define orbit update requirements.
 - c. Generate tables of orbit parameters.
 - d. Develop spatial to frequency algorithm.
 - e. Define sample interval definition per orbit and antenna.

3.2.5.1.2.4 IF/Baseband Processing. Figure 3.2.5.1-3 illustrates the IF/Baseband conversion. The 197 MHz 1st IF signal is bandpassed filtered and amplified. A switched local oscillator is used to normalize the positive and negative doppler associated with the forward and aft looking antennas. The 8.2 MHz output of the mixer is bandpassed filtered and split into eight equal power signals in a 4:1 power splitter and four 2:1 power splitters. The intent is to partition the return doppler into four frequency bands. Each band will be filtered digitally using a Fast Fourier Transform. Key to the bandsplitting

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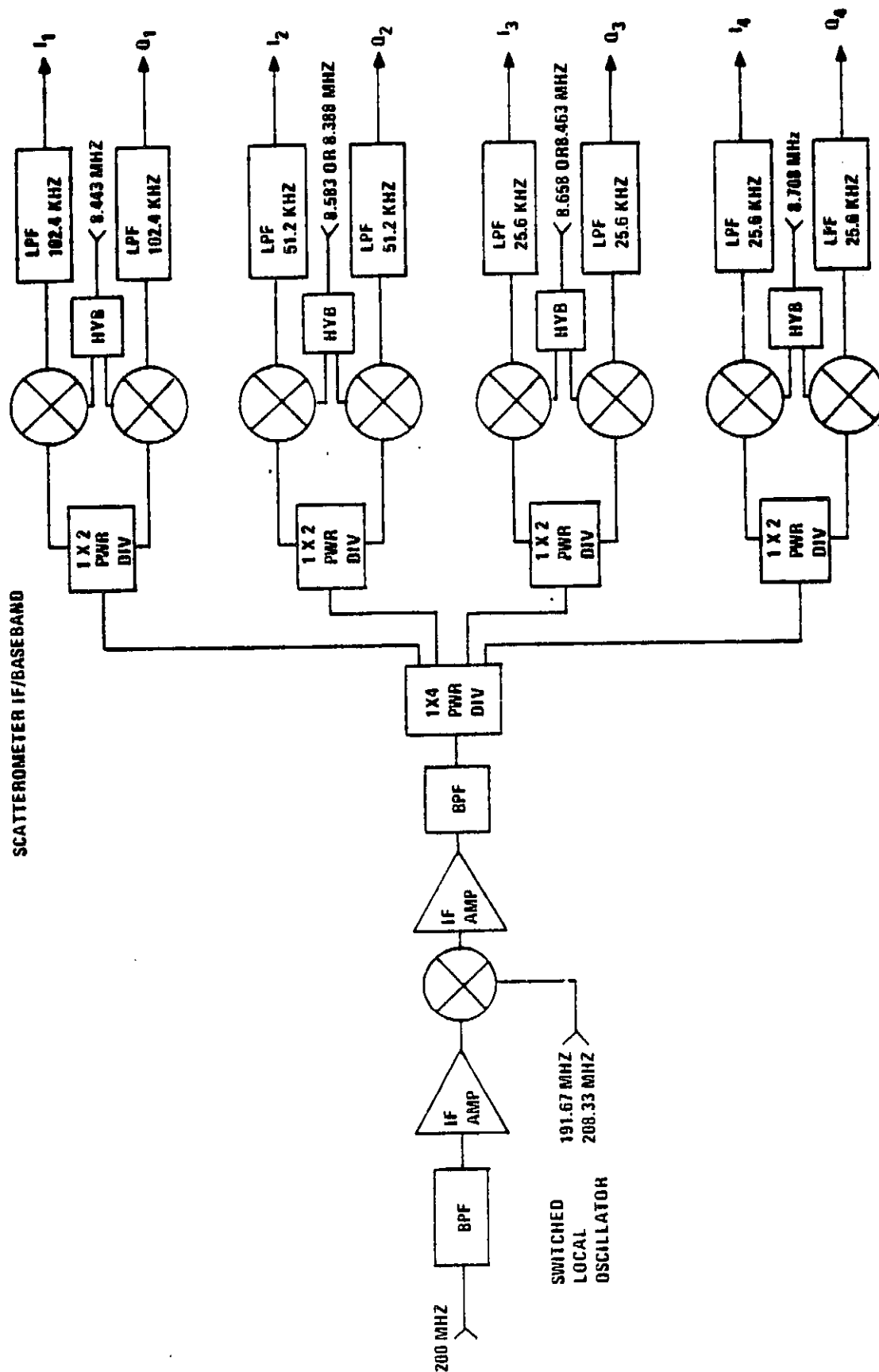


Figure 3.2.5.1-3. Scatterometer IF/Baseband

requirement is the generation of In-Phase (I) and Quadrature (Q) components at baseband. These complex waveforms (I and Q) are generated by mixing with a complex LO generated from a stable source and a 90° hybrid. The I and Q signals are low pass filtered for alias removal. These filters are critical since the maximum FFT frequency equals the cutoff frequency of the LP Filters. The doppler frequency bands are adjoining and the low pass filters must separate these bands so energy does not fold into the adjoining filters. The output of the Fourier Transform must be studied to determine which of the filter cells at the outer edge of the band be used. Normally only 70 to 80% of the transform output can be used due to out of band energy folding into the band of interest. The useful band is a function of the performance of the LP filters at the output of the I and Q mixers.

The nominal bandwidths of the four bands and associated FFT parameters are tabulated below.

<u>Band</u>	<u>Baseband Processor BW</u>	<u># Complex Samples</u>	<u>FFT BW</u>	<u># of * FFTs</u>
1	102.4 KHz	1024	204.8 KHz	4
2	51.2 KHz	512	102.4 KHz	2
3	25.6 KHz	256	51.2 KHz	1
4	25.6 KHz	256	51.2 KHz	1

*NOTE - Indicates number of FFTs performed serially in time during the return signal - PWR in corresponding Fourier Bins are summed.

These parameters are preliminary with final values to be worked out during the design phase.

3.2.5.1.2.5 Sampling and A/D Conversion. In referring to Figure 3.2.5.1-2 it can be seen that for band 1 a 256 point FFT was performed in 1.25 ms. Assuming that the timing for NROSS will be the same (a good assumption since it is mainly a function of transmit pulse width and since small deviations will not affect the conclusions drawn by this study), the time for sampling and A/D converting each sample in band 1 will be $1.25 \text{ ms}/256 = 4.833 \text{ } \mu\text{s}$.

A survey of qualified (or qualifiable) A/D converters and Sample/Hold circuits revealed that the Micro Networks MN5245 A/D converter was the fastest at 1 μ s for a 12 bit conversion and the Micro Networks MN 346 S/H with 2 μ s acquisition and settling times was adequate for the job. Using these devices, 3 μ s are required for sampling and A/D conversion. Thus the circuits are capable of handling the rates required for band 1 but are too slow to handle any additional conversions from the other bands.

However, the conversion rates of the other bands are slower so it is possible to time multiplex one S/H and A/D circuit to handle the other three bands. Since in-phase and quadrature signals are digitized simultaneously, a total of four S/H circuits and four A/D converters are required. This is less than the 8 each which were required for NOSS since at that time these fast devices were not available. The power savings are significant since the NROSS version requires about 9.7 w (including buffer amps, offset reference, and analog mux), which is about half of the NOSS number. Figure 3.2.5.1-4 shows the block diagram for the S/H and A/D functions. Note that an offset reference voltage is needed since this A/D converter only handles 0 to 5 V inputs. This results in an offset binary output code which is converted to 2's complement by inverting the MSB. The timing diagram of Figure 3.2.5.1-5 illustrates the time multiplexing of bands 2, 3, and 4.

3.2.5.1.2.6 Input Buffer Memory. During the approximately 9 ms that the return signal is present 2048 complex samples and A/D conversions are performed (4096 words total). This data must be processed by 8 FFT "batch" conversions during the approximately 16 ms between X/R cycles. A buffer memory is required to store this data. A block diagram of this memory is shown in Figure 3.2.5.1-6 for the real (in-phase) data; the memory for the imaginary (quadrature) data is identical. Parallel to serial conversion is performed by 4 shift registers. They not only provide the bit serial format required by the FFT processor but are instrumental in satisfying the timing and data permutation requirements of the FFT processor. The FFT processor requires 4 real and 4 imaginary inputs.

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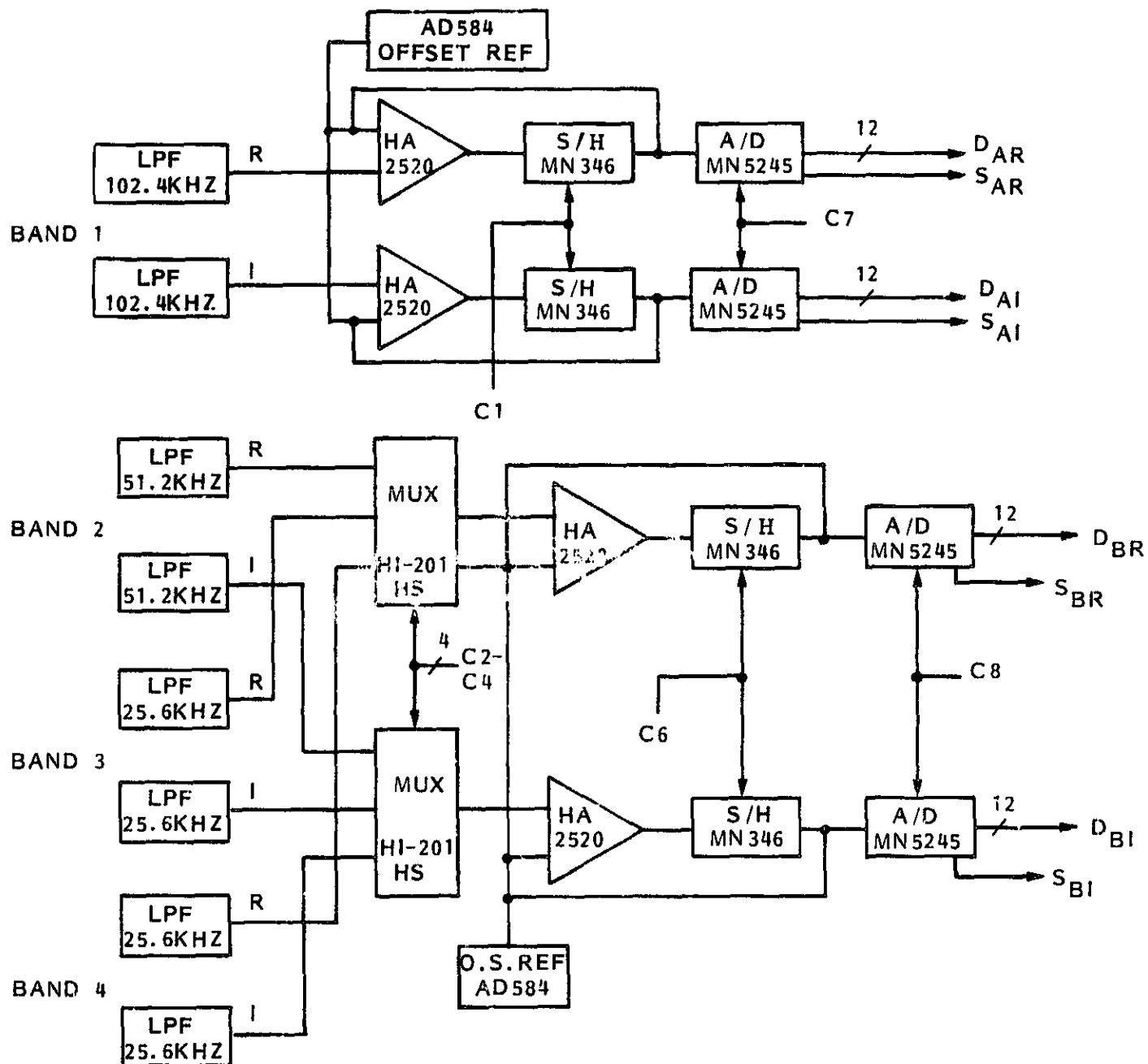


Figure 3.2.5.1-4. Block Diagram Sample & Hold and A/D Conversion

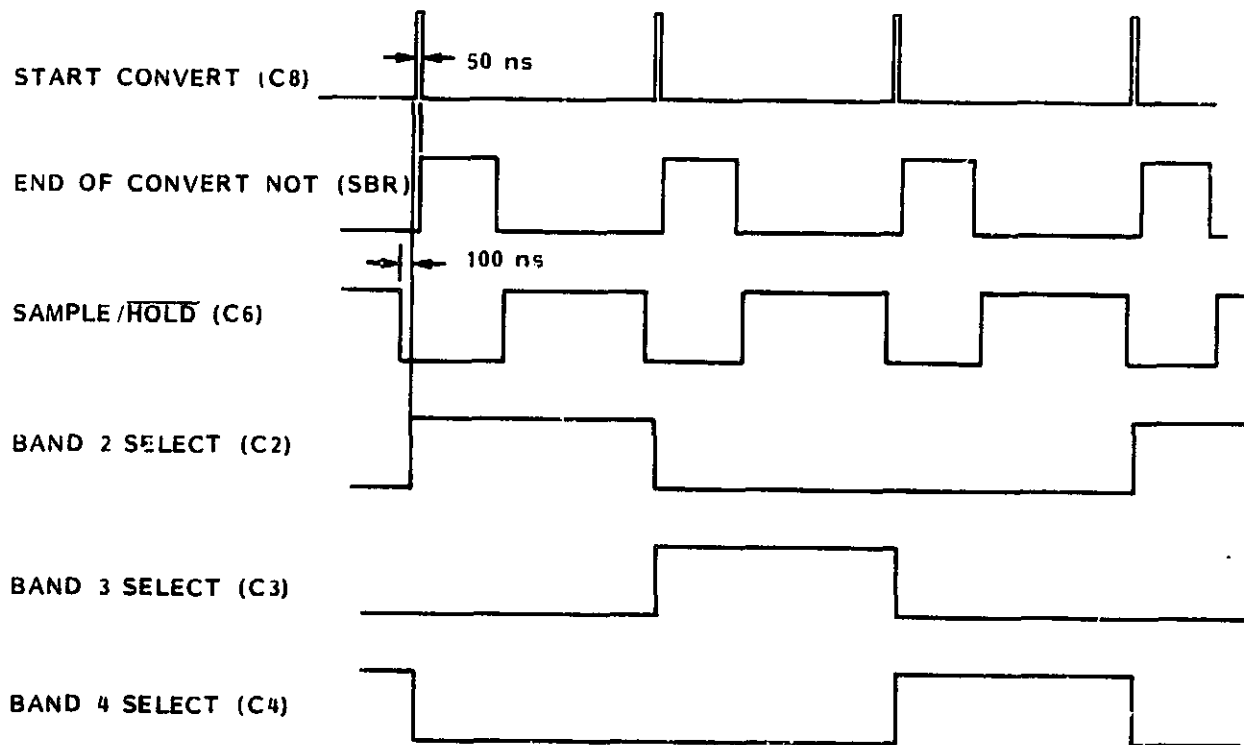


Figure 3.2.5.1-5. Timing Diagram Bands 2, 3 and 4 Multiplexing

At the expense of complicating the control logic, the buffer memory can be reduced in size since data is being sent to the FFT processor during the time some parts of memory are being filled (≈ 9 ms to fill whole memory, 2 ms to empty 1/8 th of it). However, for this study the "brute force" approach was taken and the maximum memory size was used.

Advances in the state-of-the-art made possible significant reduction in power required for this memory from the NOSS baseline. CMOS memory of adequate speed is now available and the total memory power requirement, including the shift registers for Par. to Ser. conversion, is only 1.7 w (the memory itself only needs 36 mw worst case).

3.2.5.1.2.7 FFT Processor. The FFT processor is identical to one which was breadboarded and tested as part of a GE funded IR&D program and proposed for NOSS except that the Advance Computational Element (ACE) chip is now available for

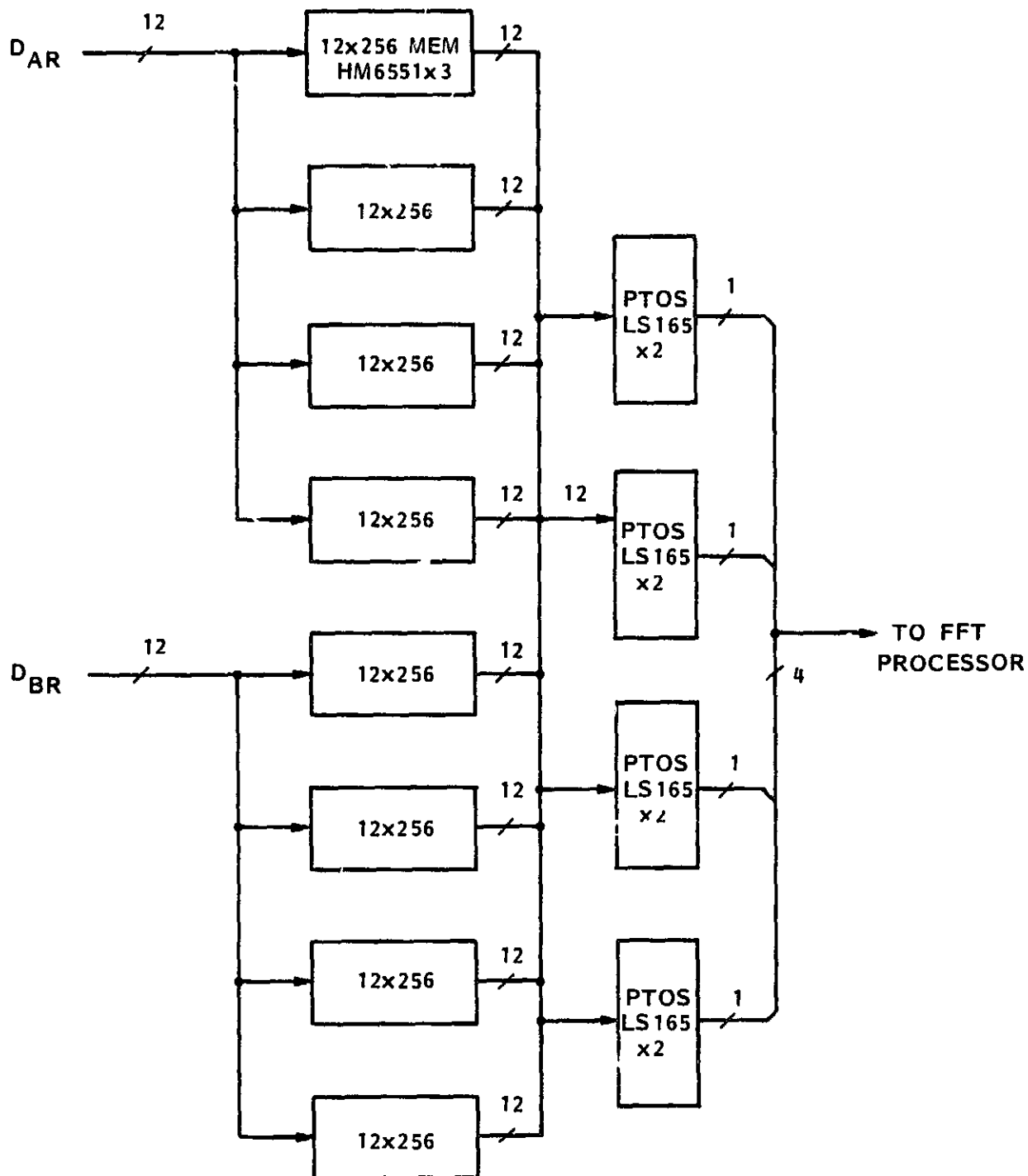


Figure 3.2.5.1-6. Block Diagram, Buffer Memory

use. The ACE is a CMOS/SOS custom LSI circuit developed and manufactured by GE. At the clock rates required for this application (2.5 MHz clock will do the 256 point FFT in 2 ms) it consumes only 6 mw of power.

A block diagram of the FFT processor is shown in the top half of Figure 3.2.5.1-7. The 256 real and 256 imaginary data words are downloaded from the Input Buffer memory through the shift registers into the FFT input memory in such a fashion that samples number 0,64,128, and 192 are the first to appear at the 4 real and 4 imaginary inputs of the computational circuit.

The computational circuit consists of 8 interconnected ACE chips. The ACE chips perform complex adds, subtracts and multiplies and are essentially in parallel except that intermediate results are cross connected between them. The data makes 4 passes through the computational chip passing from the input memory to memory 1, from memory 1 to memory 2, from memory 2 to memory 1 and finally from memory 1 to the output memory. Permutations are performed by controlling the addresses of memory read and write operations. A ROM provides the trig weights required by the FFT process. The control circuitry utilizes several PROMS to control memory addressing and data routing and timing.

The FFT algorithm used is an ordered-in, ordered out radix 4 algorithm developed by General Electric's Electronics Laboratory in Syracuse, NY.

3.2.5.1.2.8 Hann Weighting and Power Calculation Circuit. The Discrete Fourier Transform output filters are shaped as a function of $(\sin x)/x$. This shape results from the square sampling window associated with the finite number of samples ($N=256$). the Fourier transform of a pulse is $(\sin x)/x$ and the finite sampling period is mathematically equivalent to multiplication by a unit pulse. Multiplication in the time domain transforms to convolution in the frequency domain; thus, the $(\sin x)/x$ filter shape. Adjacent filter outputs crossover at approximately -4.5 dB and only 13 dB isolation exists between sidelobes. This 13 dB rejection between filters must be improved to give adequate Scatterometer performance.

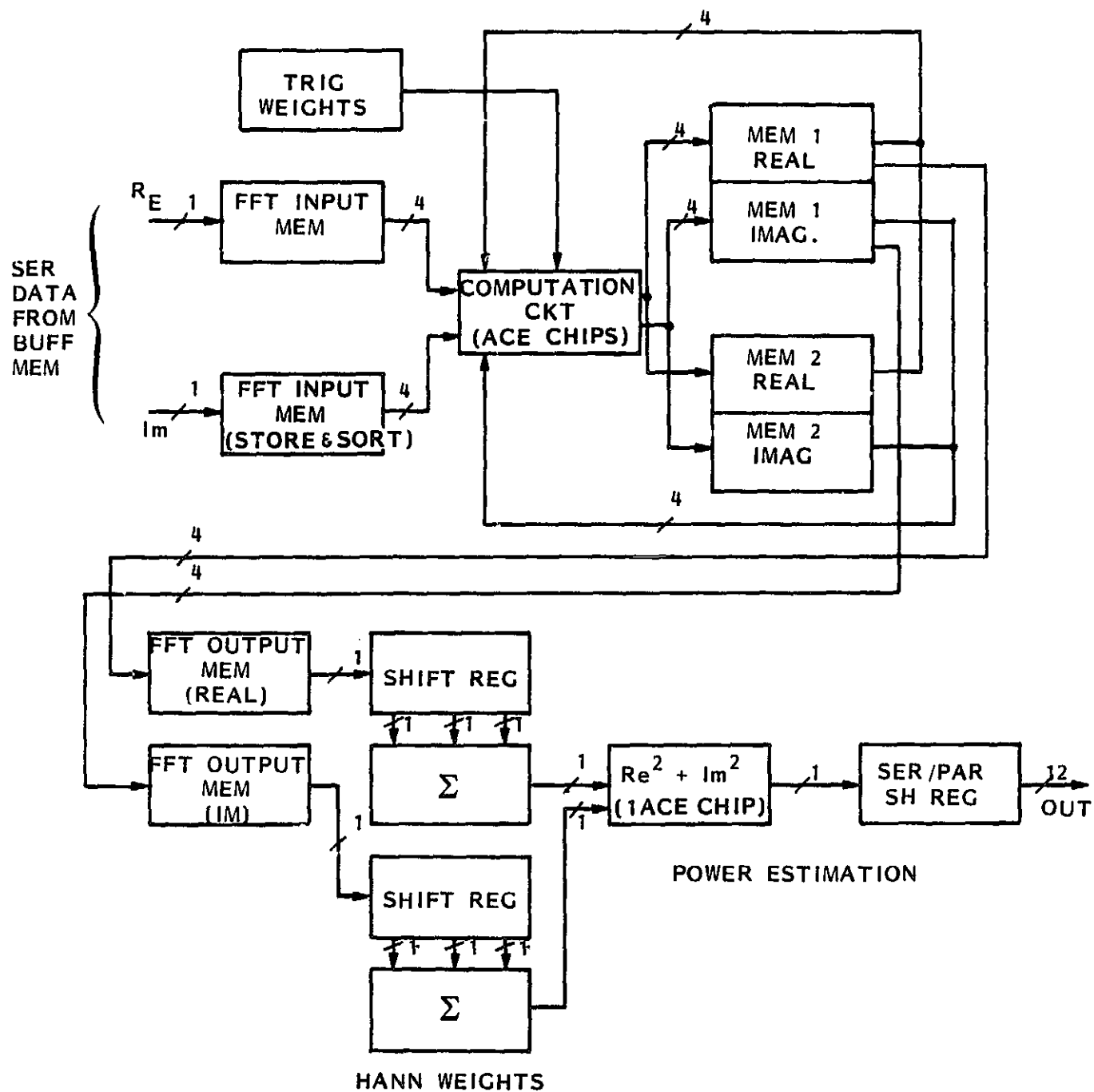


Figure 3.2.5.1-7. Block Diagram, FFT, Hann Weights and Power Estimation Circuits

Windowing techniques enable the filter shapes to be adjusted to fit desired performance. Windowing is equivalent to multiplying the input samples by some function different than the unit pulse. These functions include triangles, raised cosines, and step functions. Since multiplication in the time domain is convolution in the frequency domain, the output filter will have the shape of the transform of the windowing function.

Hann weighting is implemented by multiplying the input signal by a cosine on a pedestal. The isolation between the main and side lobes for Hann filters is greater than 30 dB as opposed to 13 dB for the uniform case.

A property of Hann weighting that makes it particularly valuable is that Hann weighting can be implemented in the frequency domain in a straightforward manner. The technique involves simple convolution (all adds and subtracts) between three adjacent bins.

The bottom portion of Figure 3.2.5.1-7 shows the circuitry needed for performing the Hann weighting. It consists of shift registers three words long tapped so as to present three adjacent words (representing adjacent Fourier frequency bins) to a summing circuit which calculates the Hann weighted output corresponding to the middle word.

The power estimation of each Frequency bin is accomplished by a single ACE chip which squares the real and imaginary components and adds the squares. A shift register is used at the output to convert to bit parallel format which is used by the subsequent co-registration circuitry.

3.2.5.1.2.9 Co-registration and Doppler Cell Accumulation. The center frequency of each Doppler cell varies as a function of Latitude as the spacecraft orbits the earth due to earth motion variations with respect to the subtrack velocity vector. Thus to insure that each Doppler cell remains at a constant crosstrack distance from the S/C subtrack position, the center frequency of each Doppler cell must be constantly changed. This is accomplished by assembling different sets of Fourier frequency bins (out of the FFT) into doppler frequency bins as a function of Latitude. This process is called Co-Registration.

With 6 antennas, 25 Doppler cells per antenna, and if the orbit is divided into 128 segments, there are $6 \times 25 \times 128 = 19200$ ways of grouping Fourier frequency bins to generate co-registered Doppler bins.

There are two basic approaches to the co-registration circuitry. One is to calculate the upper and lower frequency limits of each Doppler cell on board using the equation:

$$f_o = f_m + \Delta f \sin \left(\frac{2\pi L}{N} + \phi \right)$$

for calculating the lower limit and adding the bandwidth to obtain the upper limit.

The advantage of this method is that only 600 values need to be stored (f_m , Δf_a , Δf_d , Bw for 25 cells x 6 antennas). The disadvantage is that the algorithm cannot conveniently handle the overlap between the four bands. In order to avoid accumulating power estimates (Fourier frequency bins) from different sets of FFT's into the same Doppler cell, the four bands overlap (see Figure 3.2.5.1-2) so that the signal from a Doppler bin at the overlap shows up in the outputs of two FFT processes, but only one set is to be accumulated.

Example: If the bands did not overlap a cell could be composed of the upper 4 spectral lines of band 1 and the lower 4 lines of band 2. With overlap the cell will show up in the upper 8 lines of band 1 and in the lower 8 lines of band 2. Either one can be used for data, but if both are used the cell will show twice the actual return power.

In this method the frequency represented by each output word from the FFT processor is compared to the calculated limits to see which Doppler bin it belongs to. When the same frequency component shows up twice it is difficult to determine which one to use.

In the second method PROM's are used to store upper and lower frequency limits for each cell as a function of orbit position, antenna, and band. Referring to Figure 3.2.5.1-8, the circuit operates as follows.

The block diagram illustrates the architecture of the digital signal processing system for the Orbit Antenna. Key components and their interconnections include:

- Inputs:** ORBIT ANT (7, 3), PWR STROBE, BAND-ID (2), and FROM FFT (12).
- Memory:** PROM #1 (4K X 8), PROM #27 (4K X 8), RAM A (1024 X 5), and RAM B (1024 X 5).
- Control and Logic:** PWR STROBE, DECODE & CONT, CONTROL LOGIC, CELL CNTR, FFT BIN COUNTER, SELECTION LOGIC, COMPARE, and LATCH.
- Processing:** Two accumulators (ACCUM RAM(25 X 20)) and two summing junctions (Σ).
- Outputs:** CELL # OUTPUT (ADDRESS), S + N DATA, and N DATA (TO DATA FORMATTER).
- Connections:** The system uses various control signals like EN, MSB, and CLK, and data paths for ADDRESS (ADR), DATA, and READ/WRITE (R/W) operations. Comparison logic (A \geq B, A < B) and a WR ENABLE signal are also present.

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Before switching to the next antenna, the circuitry looks up the upper and lower limits of each Doppler cell for that next antenna at the current latitude of the spacecraft. These limits are stored in one of the Ping-Ponged memories (RAM A or RAM B) while the other memory is being used for sorting the frequency bins of the current antenna. The look-up is performed by powering up the PROMS and then selecting Doppler cells in sequence by stepping the "CELL COUNTER". At the first count of the CELL COUNTER, PROM #1 is enabled and the starting address of the first Doppler cell (address assigned to words coming out of the FFT processor, i.e., I.D. of individual spectral lines) appears at the PROM output and is latched. The control logic next disables PROM #1 and enables PROM #2 (in general terms: Disable PROM #N, enable PROM #N+1) and latches the ending address. Next, the "FFT BIN COUNTER" is cycled through 256 counts (0 through 255) and if any of the counts fall between the upper and lower limits the count of the CELL COUNTER is written as data into that address of RAM A or B (whichever is in the load mode) selected by the FFT BIN COUNTER count. Then the FFT BIN COUNTER is stepped once; this causes the 0th bit to change states indicating the next band is selected. Now the latching of upper and lower limits is repeated since the PROM address now represents Start/Stop data of the next band (2 MSB's of FFT BIN COUNTER go to 2 address bits of PROMS). The FFT BIN COUNTER is stepped through counts of 256 to 511, and the RAM is loaded as before if the count is within limits. This is repeated 2 more times to load data for Bands 3 and 4. Then the CELL COUNTER is advanced one count selecting PROMS 2 & 3 and the whole process is repeated until the RAM is loaded with data for all 25 cells.

The loading of the RAM occurs once every 627.3 ms (antenna dwell time for 25 km cells) and takes 25700 clock periods (25 cells x 1024 FFT bins + 25 x 4 latch periods). With a 2.5 MHz clock the process takes 10.28 ms for a duty cycle of 1.6%. The PROMS, latches, comparitors, decoder, and counters can all be power strobed to reduce average power requirements.

The latitude updating can be synchronized with the antenna sequencing so that the address bits of the PROM represented by these variables are not changing during the RAM loading process.

Accumulation of FFT outputs into Doppler bins is performed by 25 word wide x 20 bit accumulators. There is one accumulator for S+N and one for N only data. As the 12 bit output words appear from the FFT processor, they are accompanied by a 10 bit address. This 10 bit address is applied to the RAM which was previously

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loaded, as described above, and the RAM output is used as the address input of the enabled accumulator selecting the Doppler bin which is to receive the FFT output word. At the end of each antenna dwell period the accumulators are dumped to the spacecraft through the Data Formatter. When the data is dumped the words will be truncated to 16 bits. Although not shown in Figure 3.2.5.1-8, Ping Ponged accumulators will be used so that data can be dumped to the spacecraft concurrently with accumulation of new data.

3.2.5.2 Digital Controller

The Digital Controller is based on the SASS design and as much as possible of that design will be salvaged. However, there are changes and additions to accommodate the changes in configuration and operation. Some of the changes from SASS in terms of impact on the Digital Controller design are the extra antennas and different operating modes, changes in timing, different spacecraft interfaces, the addition of time code into the data stream and the use of the digital signal processor which requires different control interfaces and data output logic.

On previous Scatterometer programs, SASS and Skylab (S-193), the lack of a time code in the instrument data stream was found to be an inconvenience, especially for data analysis during testing at the instrument level; therefore, it is proposed to utilize the time code from the Spacecraft and insert it into the Scatterometer data stream. Containing its own synch pattern and time code, the Scatterometer data stream will be completely self-sufficient. This will allow options and fallback positions useful during spacecraft integration; for example, by using a T-cable on the data output connector (or by connecting to the test connector), the Scatterometer data could be fully recovered even if there are problems with the spacecraft telemetry system or the ground station.

The Digital Controller is expected to require five boards in the IEA assembly. The major functions of the Digital Controller are described below; refer to Figures 3.2.5.2-1 and 3.2.5.2-2 for clarification of the discussion.

3.2.5.2.1 Sequencer

The sequencer and the power-on initialize circuitry will occupy one printed wiring board. The sequencer uses a ROM to store the number of clock pulses between events and another ROM to control the state of each control signal at each event. An event is initiated when the downcounter has counted to zero from the count loaded during the previous event. A borrow pulse is produced during the L0 state of the downcounter clock setting a flip flop which enables three strobe pulses. Strobe #1 latches the event ROM data representing the updated states of all control signals at this event. Strobe #2 loads the count to the next event into the downcounter. Strobe #3 steps the address counter. When the downcounter clock goes HI the enable FF is reset disabling the strobe pulses until the next event.

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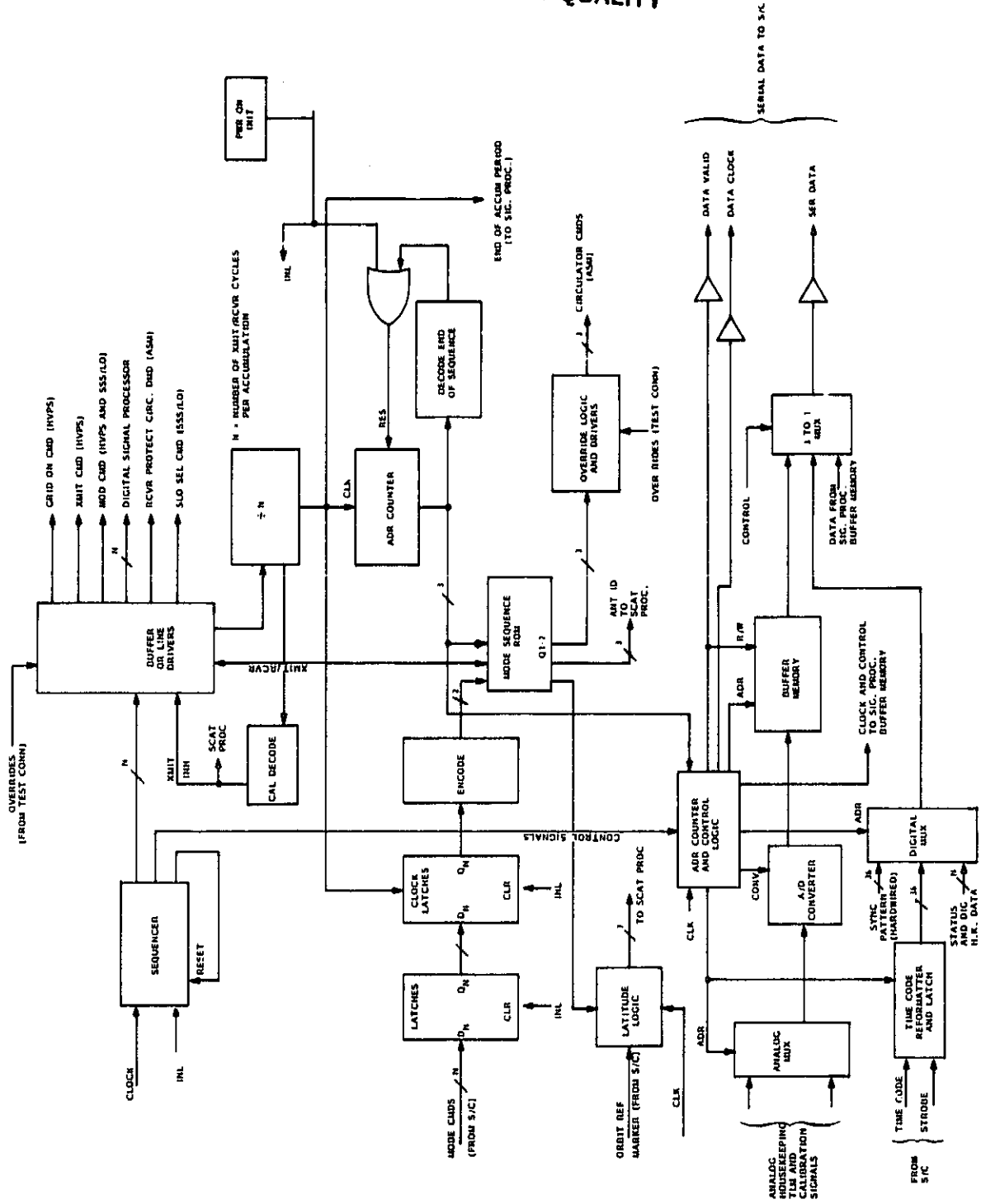


Figure 3.2.5.2-1. Digital Control Block Diagram

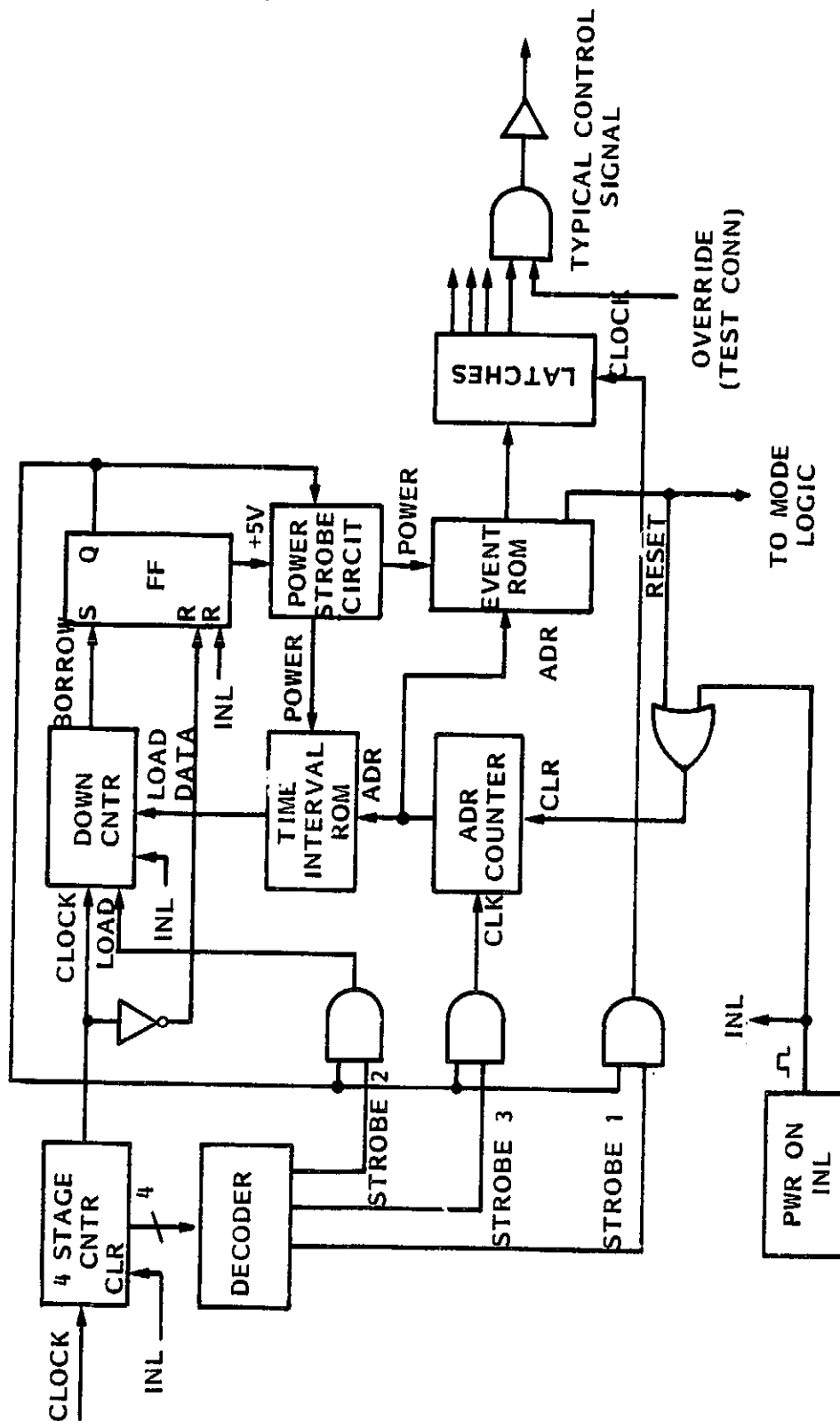


Figure 3.2.5.2-2. Sequencer Block Diagram

The granularity of event timing is a function of the period of the downcounter clock (6.4 us on SASS). The length of the downcounter and width of the time interval ROM are a function of clock period and the longest time between any two successive events. The address counter length and ROM size is a function of the number of events in a cycle. The sequencer produces the timing for a transmit/receive subcycle. The mode logic counts these cycles to generate antenna select commands. Some control signals produced by the sequencer are not used for every XMIT/REC subcycle; these are gated by signals from the mode control logic so that they occur only at the proper times (EX: Control signals for data dump to S/C, Analog & Digital Mux control, etc.).

Certain control signals require override capability via the test connector to permit testing and calibration. When the test connector is unused (open inputs) the overrides are disabled.

The ROMS can be power strobed to reduce average power, as was done on SASS.

3.2.5.2.2 Mode Logic

The mode logic will require one circuit board. This function is completely different from the SASS design. Operation is as follows.

The mode commands from the spacecraft are latched; the last command received is the mode to be executed and clears the previously sent mode. Since modes cannot be changed in the middle of a data accumulation period a second level latch is used which updates at the end of each accumulation period (when the antenna ports change). The outputs of this latch, corresponding to the modes, are encoded into address bits and select the proper area of the Mode Sequence ROM. Since the circulators in the ASM have opposite states for XMIT vs. Receive, an XMIT/REC signal from the sequencer goes to an address line of the ROM; the data in the two halves of the ROM selected by this signal are complements of each other.

The XMIT/Receive subcycles from the sequencer are counted by a counter to determine the end of an antenna sample period (data accumulation period). The output of this counter steps an address counter for the Mode Sequence ROM and the remaining address lines of the ROM are controlled by this address counter. The

outputs of the ROM are the commands to the circulators in the ASM which select the proper antenna in the correct sequence for each mode.

The circulator commands have override logic controller from the test connector to enable forcing the circulators into any configuration for test purposes. This is required for calibration and was also done on SASS. An open at the test connector disables the override.

Outputs of the XMIT/REC subcycle counter are decoded to determine when noise only data is to be taken. When the count equals a predetermined number, corresponding to "N-only" data, a comparator outputs an XMIT inhibit signal and sends a signal to the Scatterometer Processor selecting the "N-only" accumulator.

3.2.5.2.3 Analog Housekeeping Telemetry

The Analog Housekeeping Telemetry circuit will use about one circuit board. It contains the thermistor reference voltage source, precision series resistors, and an analog multiplexer for handling the temperature data required for data correction. (State of health temperature data are sent directly to the spacecraft as analog signals.) The data from this mux is subcommutated over eight data frames. Another analog mux will handle data which will be sampled once per data frame; this mux also receives the output of the temperature data mux. A 12 bit A/D converter will A/D convert the output of the mux and the data will be stored in a buffer memory. The control logic for stepping the multiplexers, controlling the A/D converter and the buffer memory are also on these boards. The sequencer sends a mux enable command to start the control logic at the proper time but the details of the control are performed by the logic. The design is virtually identical to that used on SASS except the buffer memory has been added to eliminate the gaps between words in the output data stream (as was the case on SASS) and to provide greater flexibility in designing the data interface with the spacecraft. The buffer memory eliminates the need to A/D convert at the data output rate to the spacecraft (as was the case on SASS) allowing more time for the MUX outputs to settle, resulting in greater accuracy.

3.2.5.2.4 Digital Housekeeping Logic

This circuitry will use one circuit board. It consists of a large digital multiplexer which is scanned during data dump time to the spacecraft. The first

32 to 40 inputs (depending on word size) to this mux are hardwired to +5V or ground to produce the synch pattern at the start of each data dump. Other inputs are from the time code reformatter and various bi-level and status monitors in the instrument.

The time code reformatter is a new design. It will convert the serial time code from the spacecraft to a parallel format. It will update its parallel output each time a new serial code is received. The parallel output is latched at a known point within the operating sequence of the instrument (at the start of an antenna sample period, for example) so that the time code can be precisely correlated to what the instrument was doing at the time. Logic will be designed to prevent latching the time code while it is updating.

3.2.5.2.5 Data Output Logic

This circuitry controls the selection of digital mux, buffer memory or Signal Processor buffer memory as the source of data going to the spacecraft. It will switch between these sources without glitches or discontinuities in the data stream. It will provide the clocks to these sources to keep the data bits synchronized to the data clock. It also provides control and timing signals to the Signal Processor to mark the end of data accumulation periods. It will generate a data valid (or enable) envelope and provide the interface buffers for this signal and the data and data clock outputs to the spacecraft.

Note that for costing purposes the data interface with the spacecraft is assumed to be identical to SASS and what was proposed for NROSS (except for data rate and number of bits per dump). In this interface the Scatterometer dumps data to the spacecraft in a burst when it is ready. A data valid (or enable) signal goes true (HI) before the data dump begins. The Scatterometer provides the data clock which is used by the spacecraft to receive the serial data. At the end of the data dump the data valid signal goes false. If the data interface is such that the spacecraft pulls data from the Scatterometer by providing the shift clock and enable signal the design will have to be changed to add a "ping-pong" buffer memory and sufficient filler bits to insure that no data is lost due to asynchronous operation of the Scatterometer relative to the spacecraft data system. This represents some additional cost but the difference is small relative to the accuracy of the ROM cost estimate; hence, the cost estimate is still valid.

3.2.5.2.6 Latitude Calculation Logic

This circuitry will share a circuit board with the Data Output Logic. It will receive an orbit reference marker from the spacecraft once per orbit and will calculate position on orbit by dividing the time interval between markers into TBD equal increments (probably 128 or 250 increments). This information is used by the co-registration logic of the Scatterometer Processor.

3.2.5.3 Timing & Control

3.2.5.3.1 Sensor Timing

3.2.5.3.1.1 Transmit/Receive Timing. Sensor timing is driven by orbital parameters and swath coverage requirements. For an orbit altitude of 830 Km the satellite subtrack velocity varies from 6.6498 Km/sec at the equator to 6.6341 Km/sec at maximum latitude of 81.261° for an average of 6.642 Km/sec. At this velocity it takes 3.764 sec to travel the 25 Km in-track cell dimension and since 6 antennas have to be scanned in that time the antenna dwell period is $3.764/6 = 627.3$ ms.

The timing of an XMIT/REC cycle is determined by three requirements: it must divide evenly into the antenna dwell period ($N \times t_{X/R} = t_{ANT}$), the Xmit pulse must be shorter than the minimum round trip delay from the closest cell (includes full time of the pulse), and the time from the end of the XMIT pulse to the start of the next SMIT pulse (including use time) must be greater than the maximum round trip delay.

The round trip delays are driven by the swath coverage requirements. For maximum orbit altitude of 855 Km and maximum incidence angle of 60° the maximum round trip delay from outer edge of the swath is 9.954 ms, not that these are all rough calculations ignoring spacecraft attitude errors and other minor error sources. For minimum orbit altitude of 805 Km the minimum round trip delay (to the near nadir cell at 13° nadir angle) is ≈ 5.53 ms.

For the SASS configuration the rise time of the Xmit pulse was 1 ms and the fall time 0.2 ms. For the NROSS system, however, the anticipated 1.4 droop of the

spacecraft Pulse Load Bus (providing power to the HVPS) causes a degradation of switching speed in the HVPS and a rise time of 1.5 ms and a fall time of 0.3 ms should be used for conservatism. Rounding off the maximum round trip delay to 10 ms and the minimum round trip delay to 5.5 ms the recommended timing is to have 38 XMIT/REC cycles per antenna dwell period for a cycle time of $627.3/38 = 16.508$ ms and a maximum pulse width of 5.008 ms. The timing is illustrated in Figure 3.2.5.3-1 below.

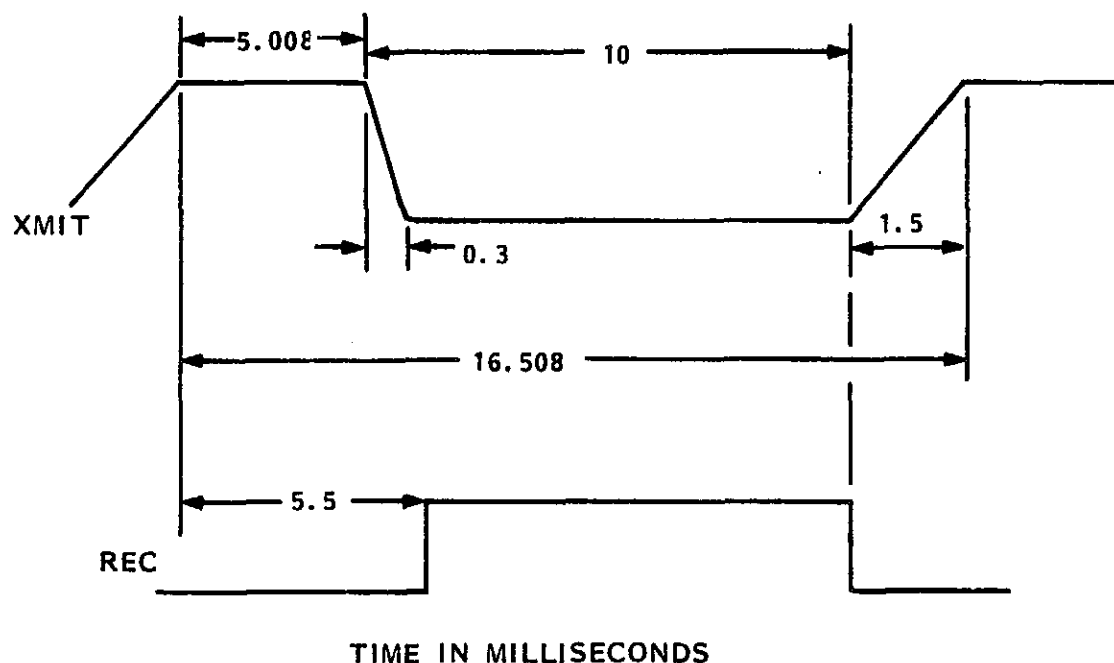


Figure 3.2.5.3-1. XMIT/REC Timing for Anticipated Pulse Load Bus Characteristics

If the Pulse Load Bus characteristics could be improved to eliminate the droop, the SASS rise and fall times could be used and 39 cycles could be squeezed into an antenna dwell period. For 39 cycles the cycle time is 16.085 ms and with a rise time of 1 ms the SMIT pulse could be widened to 5.085 ms. Assuming 2

Noise-Only cycles (re: next paragraph) the illumination time for each cell, per antenna, increases from 180.3 ms (36 x 5.008) to 188.1 ms (37 x 5.085) by use of an improved Pulse Load Bus.

Noise only measurements are made by inhibiting the XMIT pulse during some of the cycles. Further analysis will be required to determine/verify the optimum number of Noise only measurements, but extrapolating from the NROSS instrument where one Noise-only cycle was planned for 15 S + N cycles it appears that two noise only cycles out of the total of 38 is reasonable. Note that the timing developed above assumes asynchronous operation with respect to the spacecraft Data Handling Sub-system. If it is required, or determined to be desirable, to synchronize the Scatterometer to the Data Handling Sub-system the measurement cell size will need to be adjusted (from the present 25 Km size) so that the antenna dwell time and the data frame (or sub-frame) times satisfy the following equation:

$$t_{\text{ANT DWELL}} \times N = t_{\text{DATA FRAME}} \times M$$

where N and M are integers (and relatively small to minimize memory requirements). The XMIT/REC timing would then have to be re-calculated for the new antenna dwell time using the same reasoning as above.

Figure 3.2.5.3-2 shows the relationship of XMIT/REC cycle to antenna timing.

3.2.5.3.1.2 Calibration Timing. The Scatterometer instrument is calibrated periodically by connecting the Receiver to a calibrated noise source instead of the antennas. To simplify the control logic and data reduction the calibration period lasted for a whole measurement call period (time to scan all antennas once) for the SASS instrument, and is one of the possible scenarios for NROSS. However, the possibility of doing calibrates more often but only during antenna #2 & 5 dwell times has the advantage of not losing data while calibration is being performed.

From SASS experience it is known that a 4 minute interval between calibrate cycles is ot too long and that a 32 to 1 ratio of measurement to calibration time is adequate. Further analysis is required, however, to optimize the instrument with respect to calibration time vs. instrument time and the ROM costs

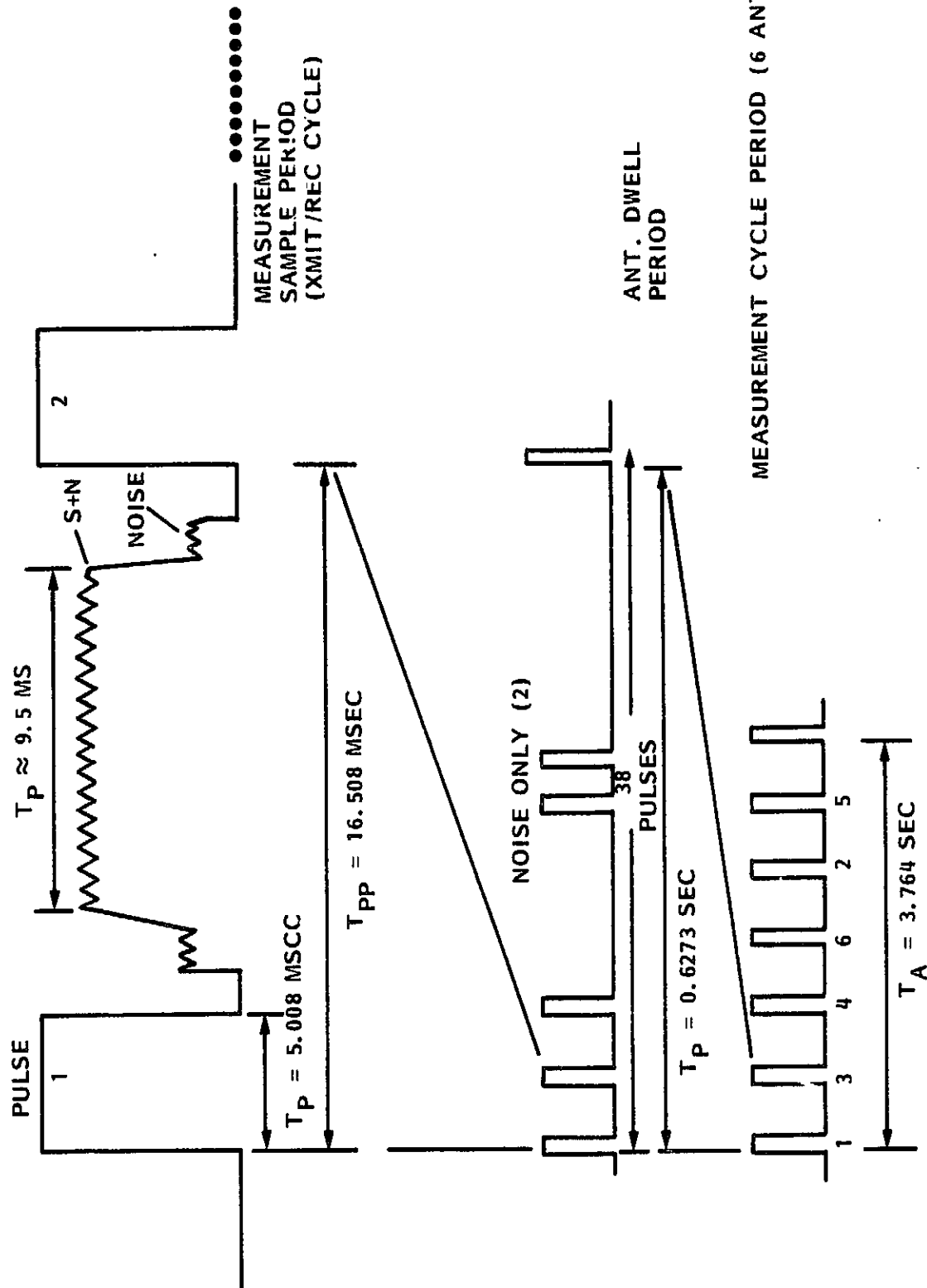


Figure 3.2.5.3-2. Scatterometer Timing Intervals

reflect this analysis. Pending this analysis some guesses can be made and some "straw man" scenarios suggested. some possibilities are:

1. One 3.764 sec calibration cycle (one measurement cell time) every 64 measurement cell times or once every 240.896 sec (approximately 4 minutes).

This gives a calibration interval same as used on SASS but the ratio of measurement time to calibration time is 64 to 1 and data is lost for every 64th cell.

2. One 3.764 sec calibration cycle every 32 measurement cell times or once every 2 minutes.

This gives a measurement to calibration time ratio equal to that used on SASS but data is lost twice as often and calibrations are only 2 minutes apart.

3. Two 0.6273 sec calibration cycles (during antenna #2 and antenna #5 dwell times) every 16 measurement cell times.

This will give the same measurement time to calibration time ratio as SASS and no data would be lost since antennas 2 & 5 are only used for ambiguity resolution and periodic loss of this data could be compensated for in the data processing algorithm.

3.2.5.3.1.3 Data Processing & Data Dump Timing. During one XMIT/REC cycle (16.508 ms) eight 256 point FFT's are done on the return signal. The return signal is digitized (sampled and A/D converted) and held in buffer memory until the FFT processor is ready for the data. It takes 4160 clock pulses per FFT process plus some TBD overhead to move data into & out of the processor thus a clock of ≈ 2 MHz is required for processing 8 sets of FFT's during one X/R cycle. The data from each X/R cycle is accumulated and dumped to the Spacecraft at the end of each antenna dwell period (once every 627.3 ms).

3.2.5.3.2 Processor Control and Data Buffers

The Scatterometer has its own control logic which sequences the instrument thru its operating cycles as a function of mode selected. The only external references required are an orbit reference marker and a time code and possibly data subsystem timing references if the Scatterometer has to be synched to the telemetry data frame (this option was not costed).

The instrument contains data buffers for holding digitized return signal data until the FFT processor is ready for it and various data buffers interval to the digital Scatterometer Processor. Any data buffers required for the data output interface to the spacecraft are not costed since the NROSS and SASS designs (assumed to be the baseline for this effort) did not require a buffer; these designs dumped data to the spacecraft directly from the accumulators asynchronously with data frame timing.

3.2.5.3.3 Telemetry and Command

The commands required by the Scatterometer and the details of the command interface are described in Section 3.2.1.3.

Telemetry is divided into two major groups:

1. Instrument state of health telemetry is provided to the spacecraft as individual analog signals (temperature monitors) or bilevel signals (relay states). This telemetry is powered from a switched telemetry bus, has isolated return, and is operational even if the Scatterometer is powered down. Details are specified in Section 3.2.1.7.
2. Science and calibration data is sent to the spacecraft serially and the characteristics of this interface are defined in Section 3.2.1.6.

3.2.5.4 Low Voltage Power Supply

The voltages needed by the various Scatterometer components are supplied by a DC/DC converter located in the Integrated Electronics Assembly. The design is basically the one flown on the SASS program but scaled up for greater power handling capability.

The DC/DC Converter accepts $28 \pm 2\%$ VDC spacecraft regulated power and produces $\pm 15\text{V}$ and $+28\text{V}$ DC outputs and a 4 volt isolated AC used by the HVPS. Conversion efficiency is 75%. figure 3.2.5.4-1 shows the various loads of the DC/DC converter.

3.2.5.4.1 Input Requirements

The DC/DC converter will be designed to operate with the $+28\text{VDC}$ Main Bus as specified in Section 3.2.1.1.1 of this document. The Main Bus Return will be isolated from all other grounds by 100 K ohms min. The loading of the $+28\text{VDC}$

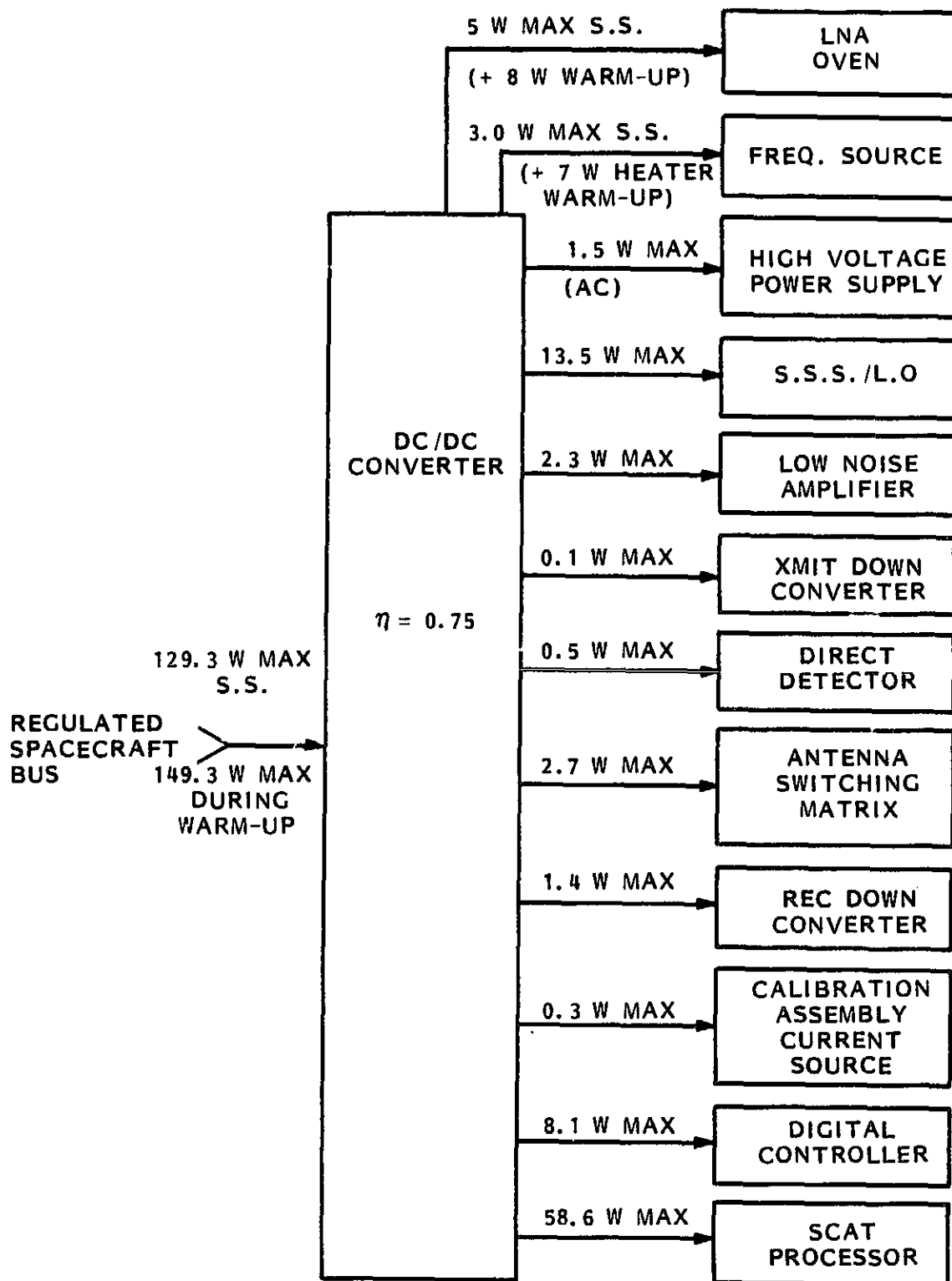


Figure 3.2.5.4-1. DC/DC Converter Power Flow Summary

Main Bus by the DC/DC converter will be as specified in Section 3.2.1.1.1. Note that the power consumption specified in 3.2.1.1.1 is slightly higher than the steady state and peak power shown in Figure 3.2.5.4-1; this is to allow for array contingencies or any items missed by this limited study. Section 3.2.1.1.1.1 should be used for developing spacecraft requirements.

3.2.5.4.2 Output Requirements

On SASS the DC/DC converter provided $\pm 5V$ at $\pm 7\%$ tolerance and $\pm 15V$ at a $\pm 1\%$ tolerance and $+28V$ at a $\pm 1V$ tolerance. The required tolerances for NROSS are not fully defined at this time; we know that the logic will work at $5V \pm 10\%$ and that for most of the $\pm 15V$ applications a $\pm 5\%$ tolerance is sufficient. Thus it appears that the basic SASS design will be more than adequate.

Output voltage ripple will be 0.6% RMS max. for broad band ripple and 0.35% RMS max. for narrow band ripple between 800 KHz. Secondary voltage returns are common to chassis and signal grounds but isolated from all other grounds by 100 ohms min.

3.2.5.4.3 Design Approach

Figure 3.2.5.4-2 shows the typical circuit design approach that will be used for the DC/DC Converter power supply. A Jensen oscillator circuit is used to convert the regulated input voltage to the required levels. An input filter with bleed resistor and split relay contacts is provided to control turn-on current transients and to protect from voltage transients. The output of the filter is chopped at a 20 KHz rate by the Jensen oscillator. Isolation between input power ground and output power returns (which become signal grounds) is provided by the output transformer. In addition, the four volts AC supplied to the High Voltage Power Supply is isolated from both power and signal grounds.

The converter will be packaged into the same relative area as the Seasat A design; but, because of the greater power handling requirement, it is allotted twice as much volume.



3.2.6 ELECTRICAL GROUND SUPPORT EQUIPMENT (GSE)

The electrical Ground Support Equipment for the Scatterometer consists of one Bench Check Unit (BCU), Return Signal Simulator (RSS) and some special test equipment. The BCU includes a Mini-Computer System for data processing, long term trend analysis and some control functions for automated testing. The BCU is packaged in standard two-bay electronic equipment cabinet.

3.2.6.1 Bench Check Unit (BCU)

The BCU is the primary equipment used for checkout and verification of the Scatterometer. It provides all electrical interfaces - power, monitoring and control. The BCU provides for continuous monitoring of input signals from the Scatterometer to verify proper performance and to insure safe operation. Figure 3.2.6-1 shows the basic block diagram of the BCU equipment contained in the two-bay cabinet. In addition to this equipment, there are two separate strip chart recorders and the BCU mini-computer equipment. Figure 3.2.6-2 shows a front panel layout of the basic BCU cabinets and Figure 3.2.6-3 shows the basic mini-computer equipment layout. The detailed descriptions of the panels of the cabinet and their operation and interfaces are included in the following paragraphs.

3.2.6.2.1 Time Code Generator

The Time Code Generator generates the 36 Bit Time Code required by the Scatterometer for use in data processing and control. This Time Code Generator is an existing commercial item that can run on either its own internal reference or an external reference. In addition to providing the 36 Bit Time Code, it provides a Low Rate Time Code for use on marker pens of the strip chart recorders of the BCU. The Time Code Generator provides a front panel indication of the time including day of year, hour of day, minute of hour and second of minute that is useful when taking test data. Front panel controls are provided for setting the time.

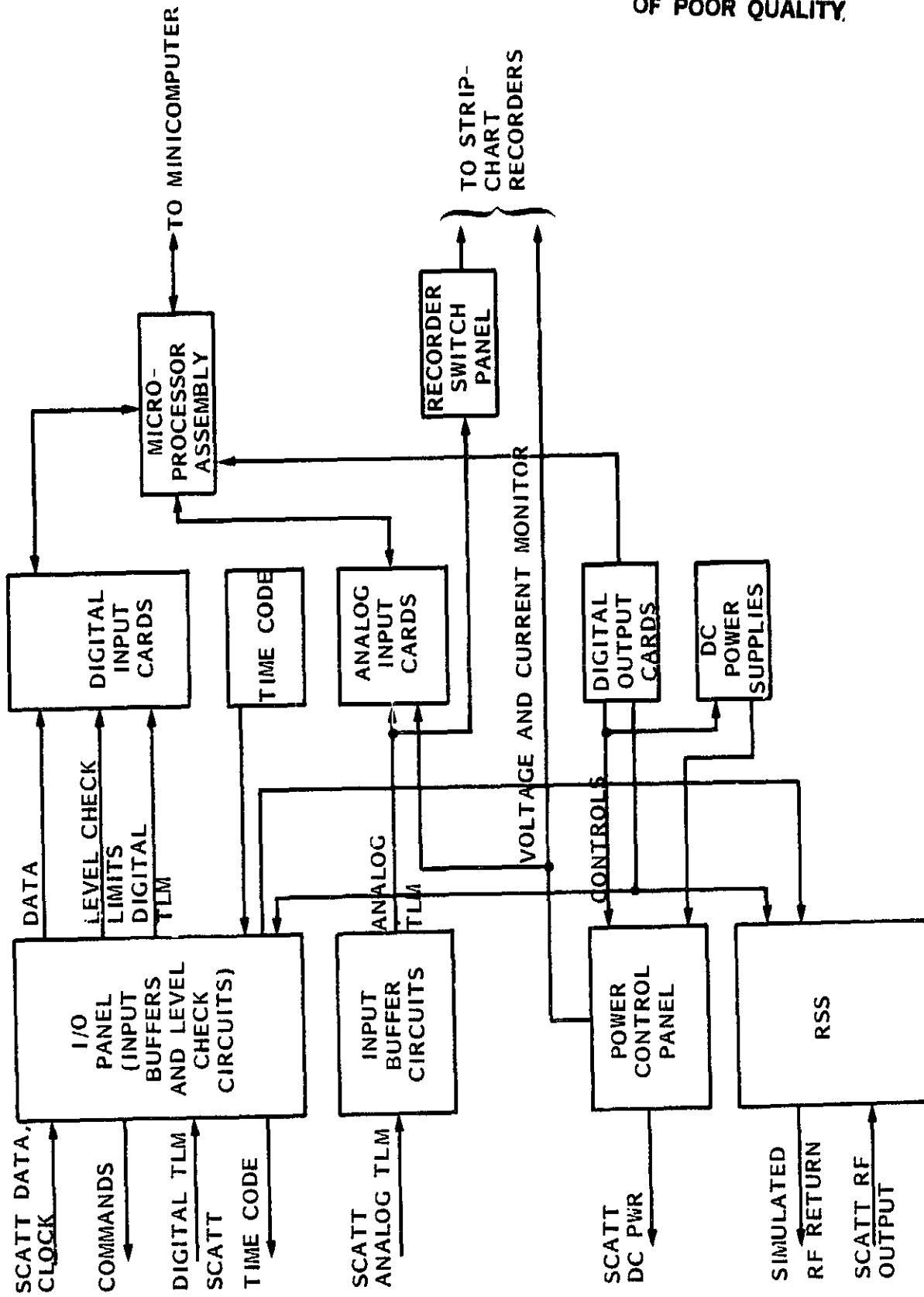


Figure 3.2.6-1. BCU Block Diagram

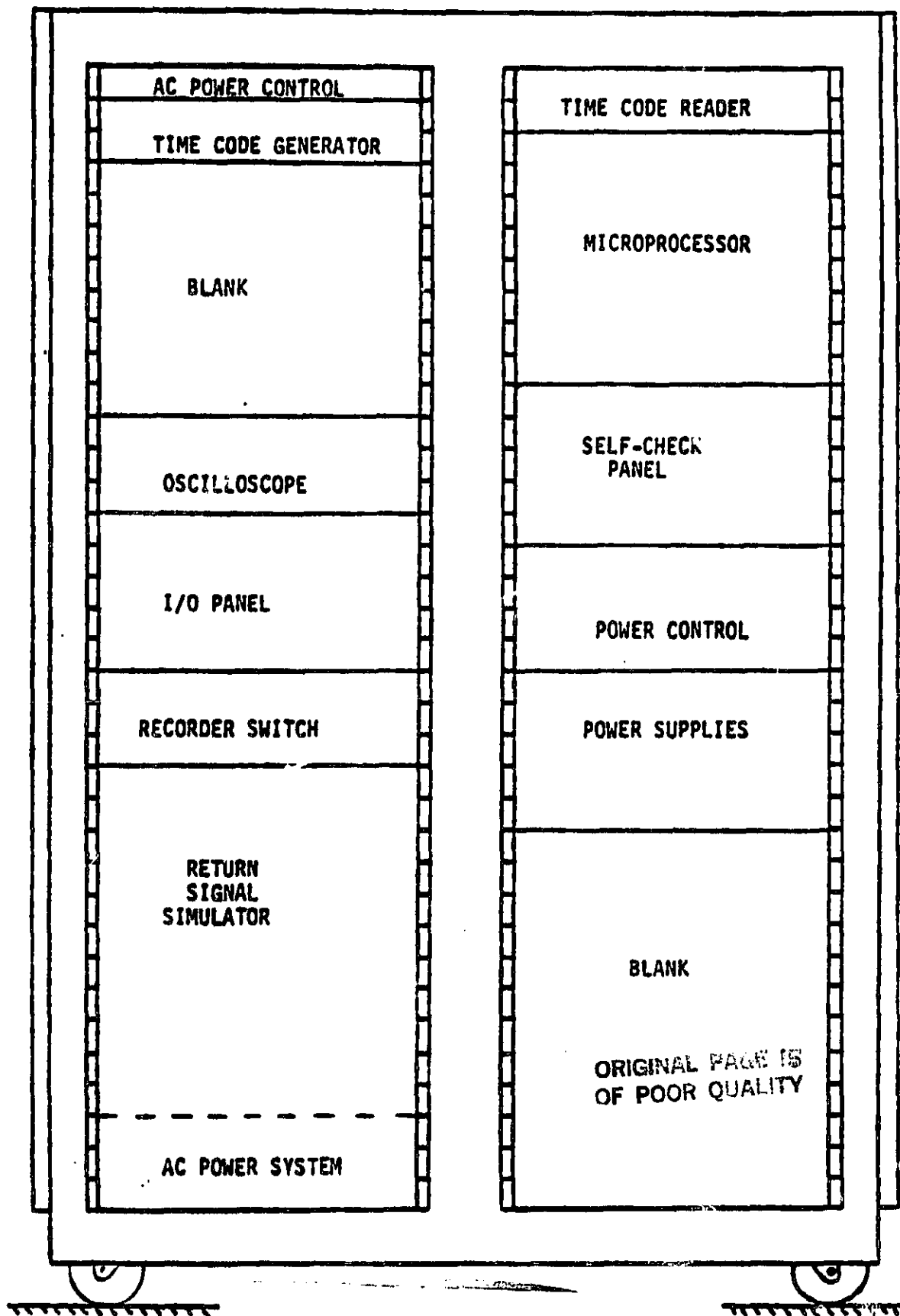
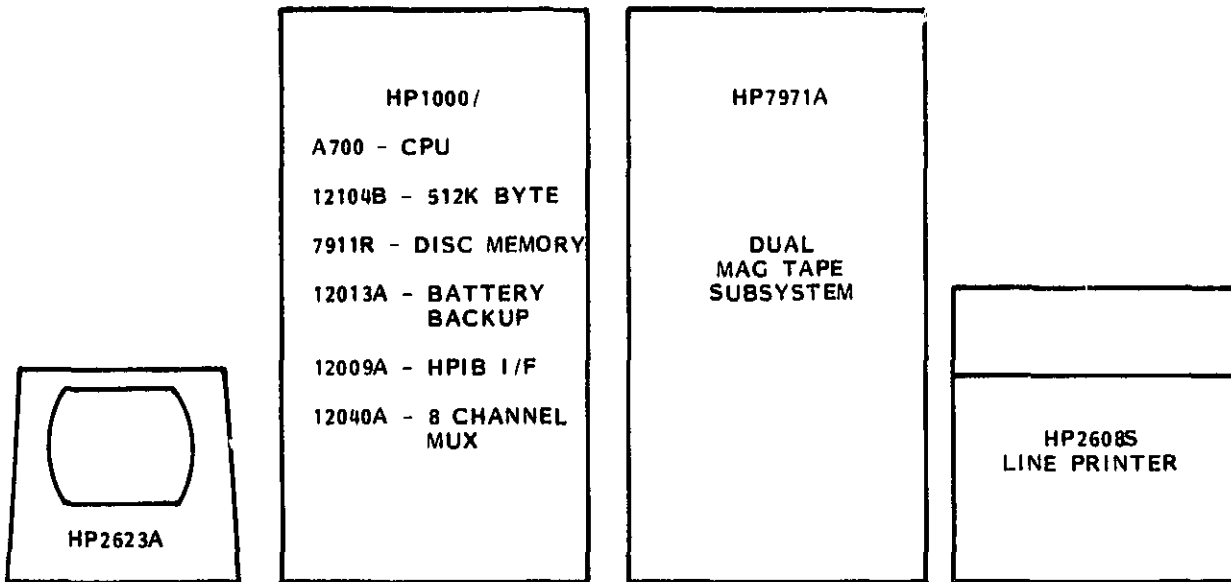


Figure 3.2.6-2. NROSS Scatterometer Bench Check Unit (BCU)

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Figur. 3.2.6-3. BCU Minicomputer

3.2.6.2.2 I/O Panel

The I/O Panel provides all interfaces with the input and output signals from the Scatterometer and is electrically identical to the Spacecraft Interface. For all digital input lines to the panel, the panel buffers the signals and compares the logic levels to high and low limits. Out-of-tolerance limits are flagged and sent to the micro-processor to indicate out-of-tolerance conditions. The limits used for this comparison are adjustable and front panel test points are provided for each input signal. The micro-processor displays the out-of-tolerance limits and merges the data with other data for transfer to the mini-computer. The incoming Scatterometer data is approximately 1.4K Bits per 627 ms Antenna Period; they are received serially and are transferred to the micro-processor. The micro-processor provides all buffering required and provides a display on its CRT of selected data words.

Signal conditioning circuits are provided for monitoring of analog temperature sensors from the Scatterometer. The buffered outputs of this signal conditioning are sent to an A/D card of the micro-processor for display by the micro-processor's CRT and for merging with other data for transfers to the mini-computer. A front panel rotary switch and digital panel meter are provided for local monitoring of the conditioned temperatures.

Interface buffers are provided for bi-level telemetry signals from the Scatterometer. These buffered signals are transferred to the micro-processor and are also displayed on the front panel via LED indicators. Analog telemetry signals are also received, buffered and sent to the A/D converter of the micro-processor for monitoring. A front panel switch and digital panel meter are provided for selecting and monitoring the analog telemetry signals. The analog signals are also routed to the recorder switch panel where they can be selected in groups to provide a hard copy on the strip chart recorder. Figure 3.2.6-4 shows a block diagram of the I/O panel output signal functions.

The Panel also provides the electrical interface to the Scatterometer for all input signals except dc power. To accomplish this function, it is electrically identical to the NROSS Spacecraft Interface. It provides the control inputs to the Scatterometer in three modes of operation:

1. Front Panel (manual) control.
2. Remote Control (via mini-computer).
3. Both manual and mini-computer control.

A front panel selector switch is provided to control which mode is active and to lock out the unwanted mode. Front panel commands are initiated by front panel backlighted switches that indicate the status of commands sent either manually or remotely. Some commands require interlocks for proper operation so logic for this function is provided in the panel. To verify proper operation of the Scatterometer with marginal interface signal levels, three adjustable signal levels are selectable via front panel controls. These levels (adjustable via trimpots internal to the panel) allow the nominal pulse levels as well as the high and low limits to be selected. Buffered front panel test points are provided for all output commands.

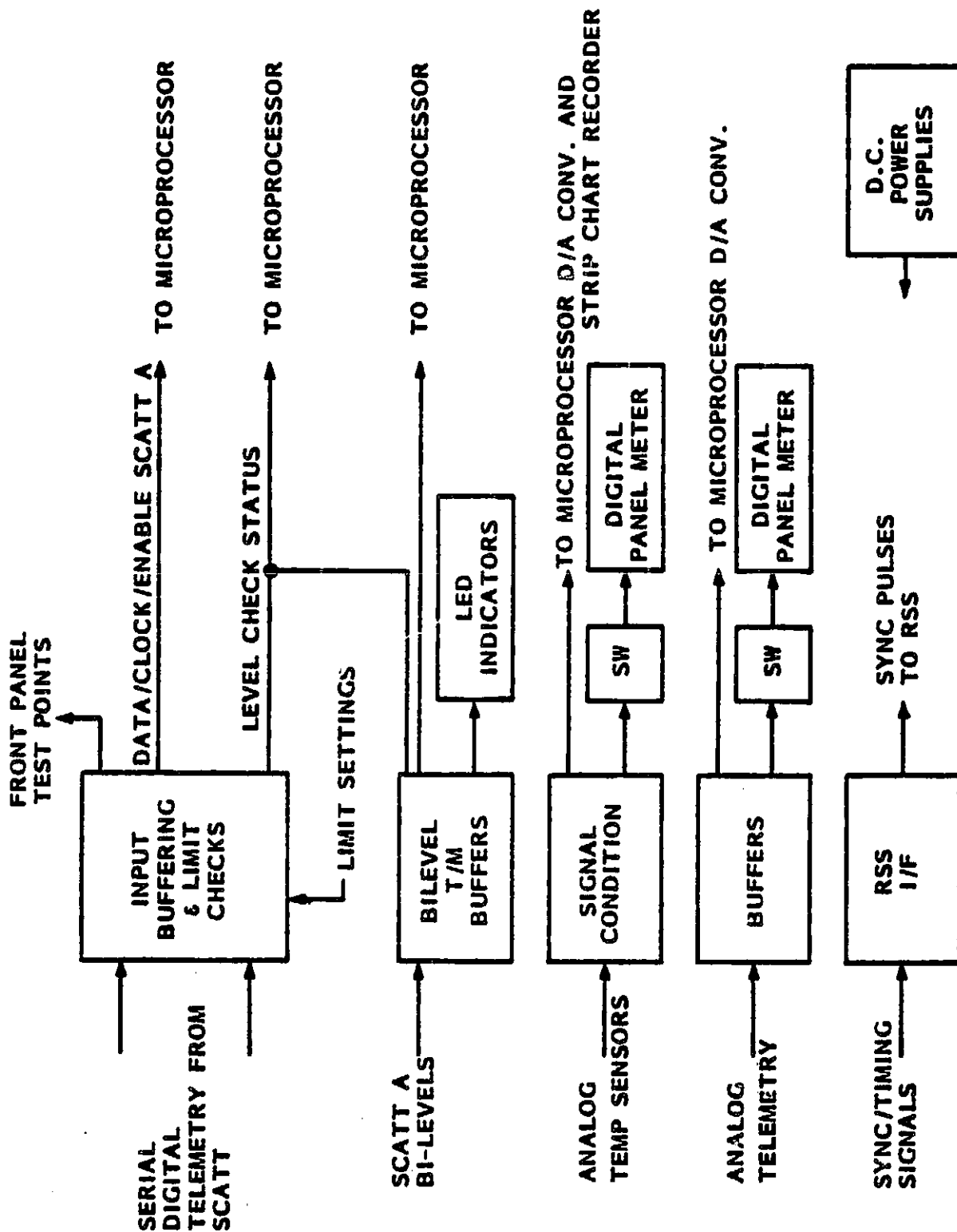


Figure 3.2.6-4. I/O Panel Output Signal Functions

This panel also simulates the 60 antenna thermistor inputs to the Scatterometer. A selector switch under front panel or remote control selects one of the 60 thermistors for simulation and a second switch (also under front panel or remote control) selects one of 10 values for the simulated thermistor. Test points are provided for monitoring the value of the simulated thermistor at each interface.

In order to keep an accurate measure of the running time on the Scatterometer components, the Input Interface Panel provides running time meters. These meters are controlled by either manual or remote commands to the components. Figure 3.2.6-5 shows a block diagram of the I/O Panel, input signal functions.

3.2.6.2.3 Power Control Panel/Power Supplies

The Power Control Panel and Power Supplies provides dc power to the Scatterometer, controls the input voltages, monitors for overvoltage, undervoltage, and overcurrent limits, conditions the monitor signals and provides the safety features required to protect the Scatterometer and the BCU. Figure 3.2.6-6 shows a block diagram of the power supply and the power control panel. This panel and the power supplies provide two primary busses to the Scatterometer of regulated power from +27.4 to +28.6 volts and a buss of unregulated power from +24.0 to +32.0 volts. Figure 3.2.6-6 shows essentially 1/2 of the total required power equipment. The dc power supplies provide sufficient capacity to handle the full transient current required while the Scatterometer TWT is on, but do not provide the capability to simulate ripple or voltage spikes. The power supplies have an external voltage adjust input from the power control panel where the output can be adjusted from either the front panel or remotely from the micro-processor. The power supply output voltage is remotely sensed just before connection to the Scatterometer to insure good voltage regulation. The power supply output is routed through the power control panel where a current shunt and signal conditioner are provided to monitor the output current to the Scatterometer. The output current is monitored by a dedicated meter and also monitored by the strip chart recorder and the micro-processor. The bus outputs are monitored for overvoltage and undervoltage as well as overcurrent with any of these conditions causing the output breaker to remove current from the instrument. Manual turn-on of this breaker is required to reapply power. The output voltages are monitored via a dedicated front panel meter and also by the strip chart recorders and the micro-processor.

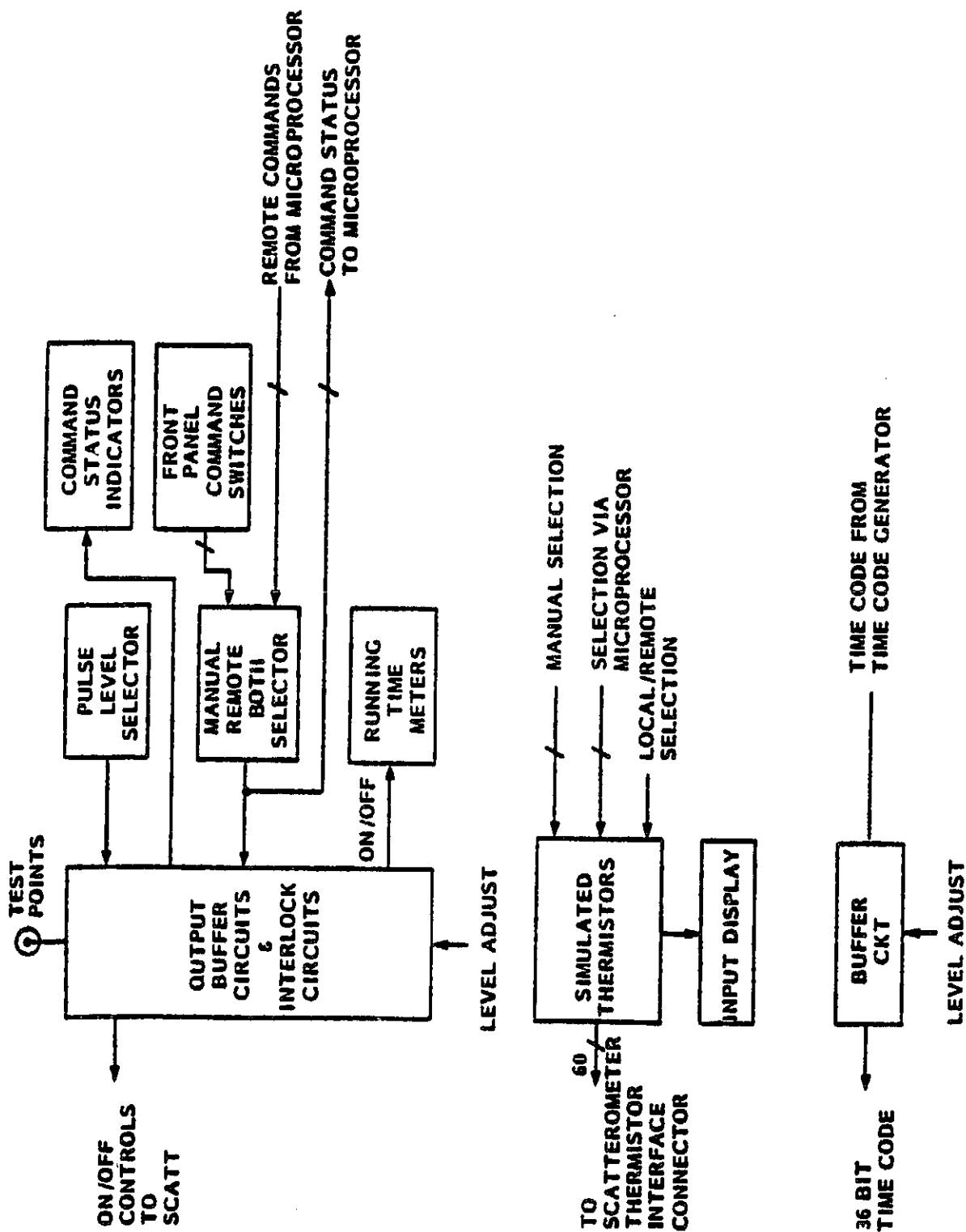


Figure 3.2.6-5. I/O Panel Input Signal Functions

- c. Stores limits for data checking, but can also update limits via the CRT or via the mini-computer.
- d. Displays operator requested data on the CRT and continuously updates this data as new data is received.
- e. Initiates an audible alarm if limits of "sensitive" parameters are exceeded to further alert the operator.
- f. Merges the telemetry data with analog telemetry bi-level telemetry, input power voltages and currents, command status and other BCU parameters to form a composite data package for transfer to the mini-computer for recording and future data analysis.
- g. Monitors the digital output word limit check circuits of the Output Interface Panel to verify that data logic levels are within tolerance.

Figure 3.2.6-7 shows a block diagram of the micro-processor.

3.2.6.2.5 Strip Chart Recorders

The two (2) strip chart recorders provided for the BCU are Brush Model 200 units each of which has eight channels of analog display and two event marker channels. The recorders are mounted in self-contained enclosures and are on wheels to permit mobility. The signal inputs to the recorders is via the BCU with one recorder used exclusively for monitoring Scatterometer dc power and currents. The other recorder inputs are selected by the recorder switch panel that allows analog telemetry signals from the Scatterometer to be selected for display via two rotary switches in banks of four channels to the recorder pen channels. One of the event pens at the edge of the recording paper of each recorder is used to record time of day to aid in data correlation.

3.2.6.2.6 Self-Check Panel

The Self-Check Panel provides the means to self-check the BCU to insure that it is functioning properly and ready to interface with the Scatterometer. To accomplish this, the Self-Check Panel duplicates the interfaces of the Scatterometer and when in use is cabled to the same interface cables. Figure 3.2.5.2-8 shows these connections. The Self-Check Panel provides simulated signals to duplicate the Scatterometer outputs. Figure 3.2.6.2-9 shows a block diagram of these functions. The serial data interface is simulated; a staircase pattern or a fixed value for each data word can be selected. If a fixed pattern

is selected, all words have the same value but this value can be selected via front panel thumb wheel switches. The simulated output, data, clock, and enable, are buffered before being transmitted to duplicate the Scatterometer electrical output.

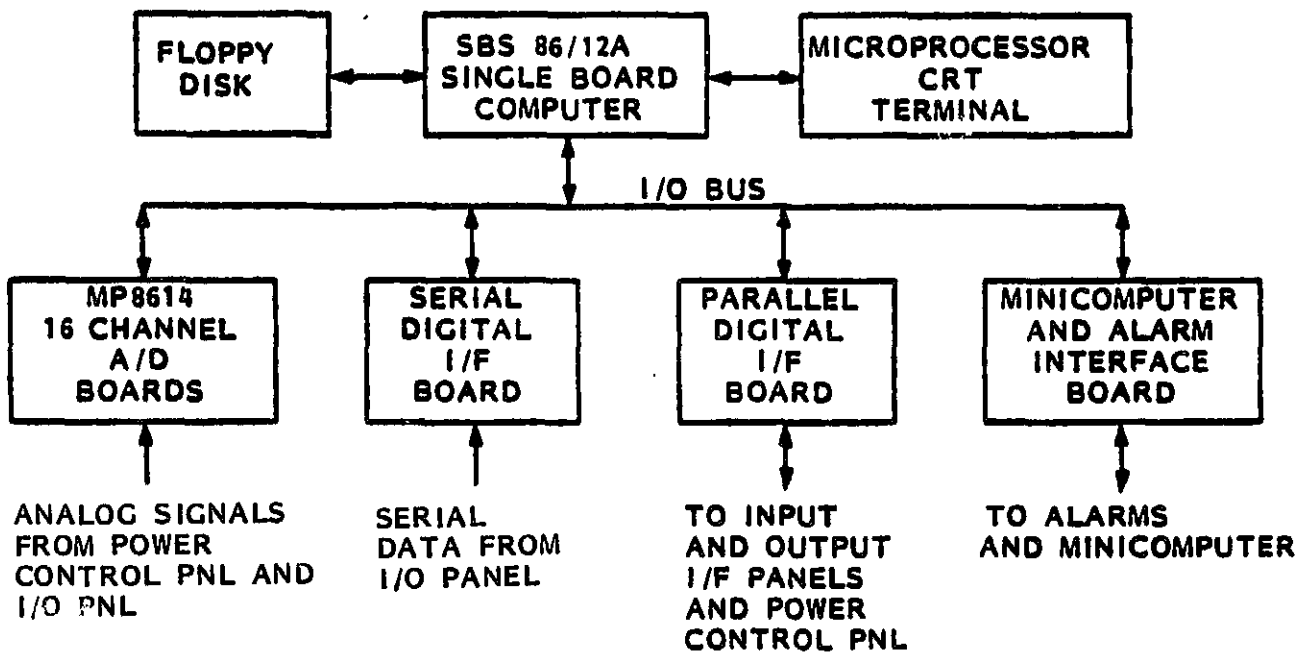


Figure 3.2.6.2-7 Micro-Processor Assembly Block Diagram

Analog telemetry signals are simulated by a selector switch and D/A converter that allows a 10 point calibration of analog output signals. Bi-level discretes are simulated individually. Bi-level output levels can also be selected via the same selector used to set the serial telemetry logic levels.

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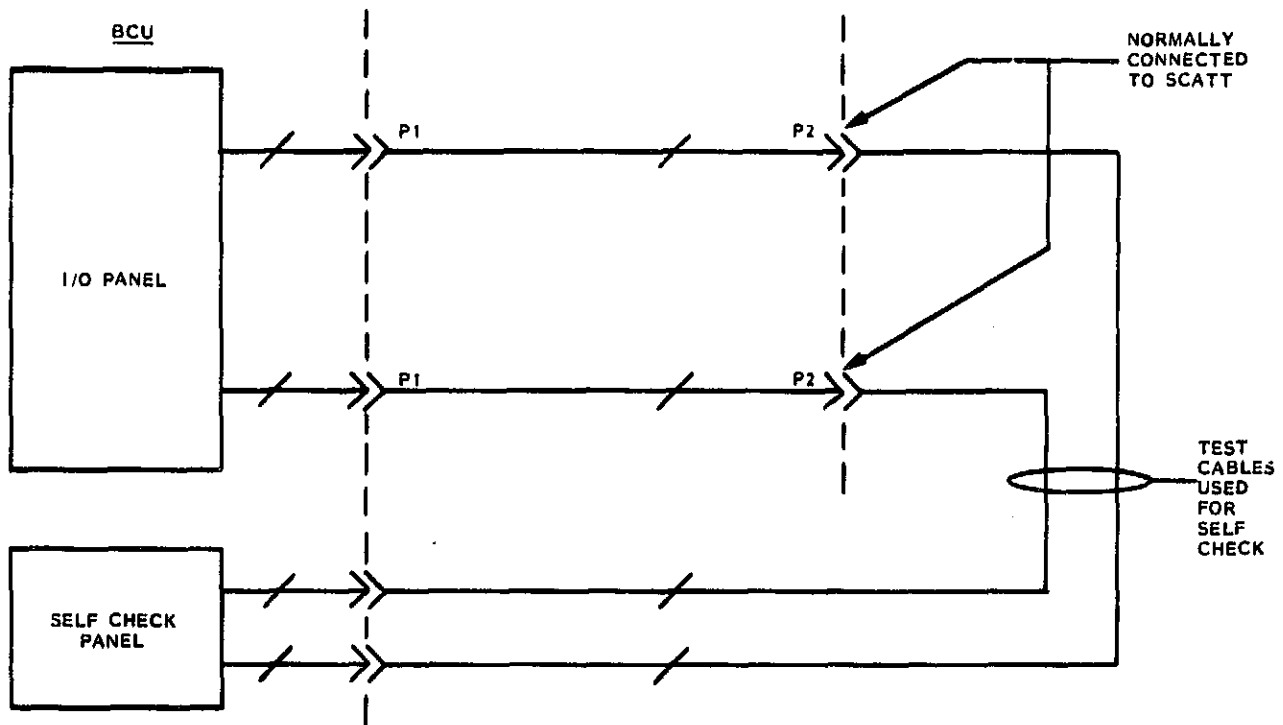


Figure 3.2.6-8. Self-Check Panel Connections

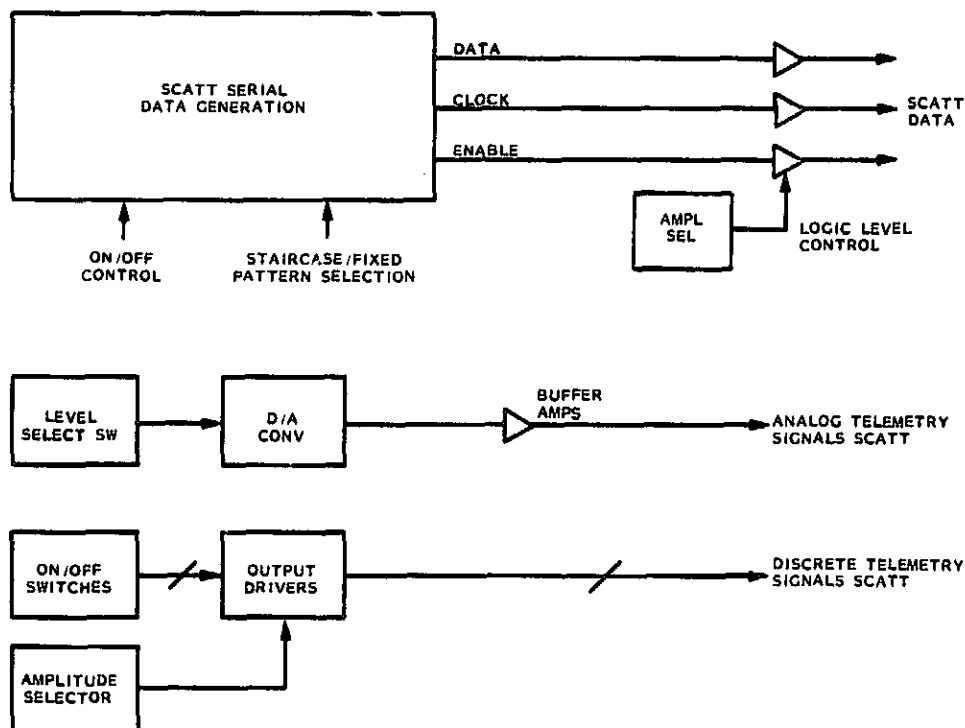


Figure 3.2.6-9. Self-Check Panel Simulation Block Diagram

The Self-Check Panel also contains circuits and displays to verify receipt of the proper signals from the BCU. This includes the following:

- a. Display of time code received.
- b. Display of discrete commands. Line receivers, test points and displays are provided for every discrete command.
- c. Monitor of simulated antenna thermistors. Test Points are provided to monitor the simulated antenna thermistors via an external ohm meter.

3.2.6.2.7 Oscilloscope

An Oscilloscope, Tektronix R7603 with 100 MHz 7A18 dual trace amplifiers, 7B53A dual time base and meter module are provided as part of the BCU for general purpose use and for monitoring Scatterometer output rf pulse waveforms via the RSS.

3.2.6.2.8 Mini-Computer

The mini-computer is part of the basic BCU. The mini-computer receives raw data from the BCU micro-processor and stores the raw data on history tapes. The mini-computer maintains a directory of history tapes that includes the data and time the test data was obtained, what procedures were being used including major paragraphs, operator names and comments, identification of the unit under test, etc. The mini-computer also plays an active part in automated tests where it, via the BCU Input Interface panel, controls the BCU and sends commands to the Scatterometer and Return Signal Simulator. The mini-computer also maintains a directory of automated tests and stores the test sequences on disk. During automated tests, the mini-computer performs real-time limit checking of Scatterometer outputs to verify that the Scatterometer is responding properly.

Playbacks of history tapes can be converted to engineering units using stored calibration and conversion parameters. Data can be displayed on the mini-computer CRT Terminal and/or printed in engineering units on the line printer. The operator has a number of options when doing this:

- a. Print all data including Scatterometer and BCU.
- b. Print all Scatterometer data.

- c. Print all Scatterometer data and changes to the BCU data.
- d. Print all data, but only if changed from the previous frame by a specific amount.
- e. Print all data, but only if changes from the previous printout by a specific amount with the amount selectable for each data value.

The mini-computer also generates corrected magnetic tapes from the raw data converted to engineering data and formatted. The mini-computer maintains a file of these corrected tapes including the identification of the raw data tape used, date, time, equipment ID under test, calibration used for the conversion, etc. The mini-computer maintains files of the calibration factors used and a directory of these files.

To evaluate performance and perform test analysis the Subsystem Evaluation Program performs the following functions:

- a. Calculates transmitted power.
- b. Calculates received power for each cell.
- c. Flags all out of spec values.
- d. Looks for anomalous trends.
- e. Calculates trends.
- f. Provides statistic functions for science and housekeeping data.

These outputs can be written to the line printer, placed on disk for later comparisons and written to magnetic tapes.

The front panel layout of the mini-computer equipment was shown in Figure 3.2.6-3. The following paragraphs describe some of the characteristics of the mini-computer hardware. A description of the software is contained in Paragraph 3.2.5.3. The CPU used is a HP1000/A100 that includes the following features:

- a. Virtual Memory for data arrays.
- b. Power fail/auto restart.

- c. ASCII console emulator allowing complete control of the computer via any ASCII Terminal.
- d. Multifunction ROM Module with ROM bootstrap loader.
- e. Hardware Floating Point multiply/divide.
- f. Multi level vectored priority interrupt.
- g. Hardware memory management.
- h. Direct Memory Access (DMA) on all I/O channels
- i. EIS (Extended Instruction Set).
- j. Automated self-test feature on power up.

The memory includes 512K bytes of error correcting memory and battery backup is provided for the memory. A 28M Byte cartridge disk is provided. A 2623A Graphics Terminal is provided for operator interaction.

HP RTE-A.1 Operating System and Fortran 77 are provided. A dual nine track, 1600 BPI magnetic tape unit. HP 7971A/OPT 144 is included with a single tape controller. The line printer is a 2608S, printing 400 lines per minute with 132 characters per line and a 128 character set.

HP Floating Point Processor is included for use with the CPU. An 12040A Async Multiplexer is included to interface with the raw data from the BCU and to interface with the I/O Panel when the BCU is under mini-computer control. A 12009A HPIB interface is included to interface with the disks and with HP test equipment.

The mini-computer supports one test at the component level of the Scatterometer. In this test, the mini-computer is used to check out and calibrate the digital filters in the Scatterometer Integrated Electronics Package. For this test, Hewlett-Packard Test Equipment with IEEE-488 (HPIB) interfaces are used which is directly Compatible with the mini-computer.

3.2.6.2.9 Return Signal Simulator (RSS)

The Return Signal Simulator allows the capability to test the RF interfaces of the Scatterometer without the antennas. The RSS is essentially a synchronously gated noise source of adjustable amplitude and a load with pulse detector and power meter coupled to the Scatterometer RF ports via multicoupler manifold. Figure 3.4.1.2-10 shows a block diagram of RSS.

Synchronizing signals from the Scatterometer to the BCU are used to gate the noise diode on and off at the proper time to simulate the return signal. The noise diode output passes through an isolator, bandpass filter, and amplifier to bring it up to the maximum value required. Two remotely controllable attenuators with a total range of 110 dB are then used to drop the noise level to the value required for the test. The two attenuators give 0 to 110 dB in 10 dB steps and 0 to 11 dB in 1 dB steps. The attenuators are remotely controllable from the BCU but also can be manually set from the front panel of the RSS. The attenuator setting is displayed when operating in either local or remote control. The level controlled output noise passes through an isolator and a circulator to get to the RSS input/output port. From here the noise is sent via coaxial cable or waveguide depending on the uncertainties allowable in the test to the cross-guide hybrid manifold that interfaces to the Scatterometer waveguide ports. For routine tests, coax is used between the RSS panel and the manifold. For critical tests including calibrations and thermal vacuum tests, the coax is replaced by a waveguide to allow more stable and repeatable tests. The manifold consists of cross-guide couplers at each port to the Scatterometer with each port connected to the manifold via a short piece of flexible waveguide and each coupler having its own load. The coupled outputs of each port are common with a waveguide load on one end and either a W/G to coax adapter on the other end or just a W/G flange (again depending on tolerances allowable for the test to be run). When the Scatterometer is transmitting a pulse, the RF energy is partially coupled through the manifold back via coax or waveguide to the RSS Panel. At the RSS Panel, the signal is routed via the circulator through two 20 dB couplers to a dummy load. One of the couplers has a diode detector so that the transmit pulse characteristics can be analyzed via external equipment - oscilloscope, counter, spectrum analyzer, etc. The other coupler feeds a power meter detector/power meter for manual readout of the Scatterometer transmit power.

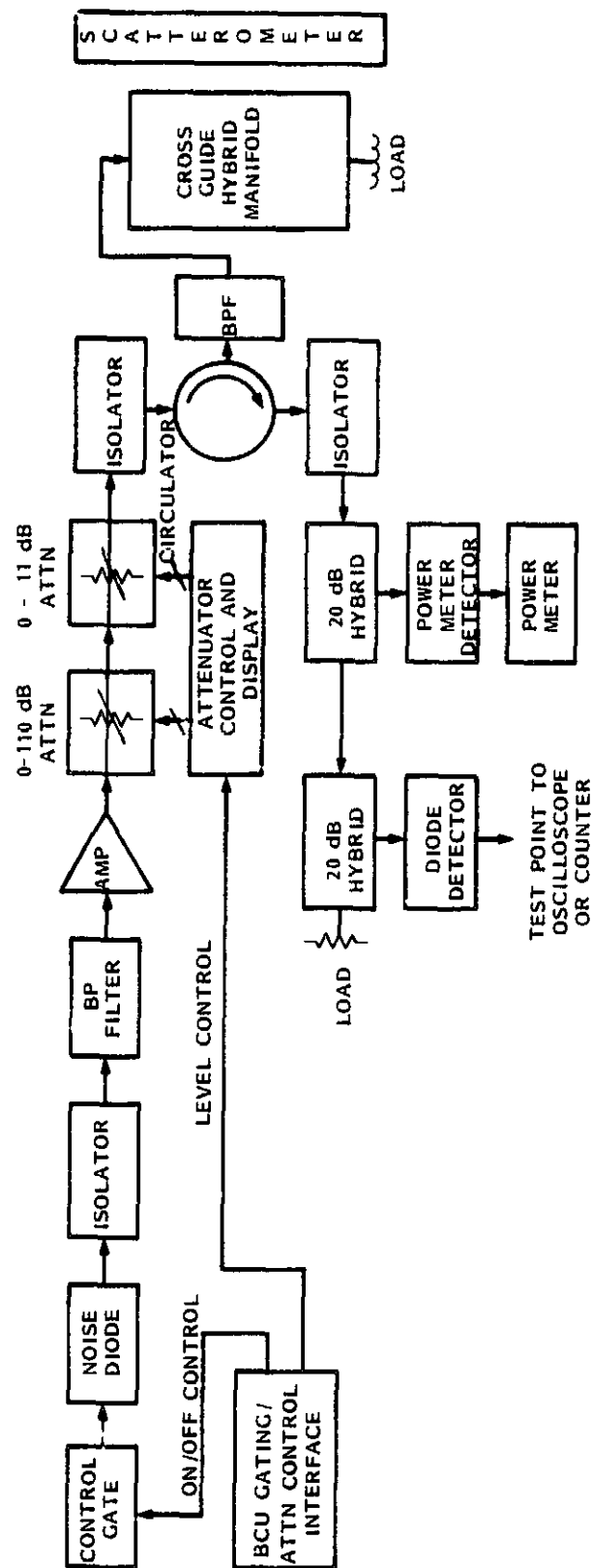


Figure 3.2.6-10. RSS Block Diagram

In addition to the RSS panel containing a power meter and the set of equipment as shown in Figure 3.2.6-10, the RSS includes the manifold of cross-guide couplers connecting to the Scatterometer, support brackets for the manifold, coaxial and waveguide runs from the panel to the manifold.

3.2.6.3 Test Software

The BCU software will be managed by a Software Project Management Plan. This plan will be the master plan for managing the software development work. The plan explains the methods and schedule for development of the BCU software. The plan also defines the implementation approach.

3.2.6.3.1 Design Techniques

The following design techniques will be used to develop the BCU software:

- a. Top-Down Approach
- b. Structured Programming
- c. Programming Teams
- d. Structured Walkthroughs
- e. Unit Development Folders

Top-Down Approach. The Top-Down Approach will organize the BCU software system into a tree structure of program modules. With this approach, the first step will be to describe a generalized structure or set of program module to solve the programming problem. These first level modules will be divided into succeeding levels of modules to form a tree-like pattern for the design and development process. Modules will be described to as detailed a level of functional definition as is necessary to produce a relatively easily understood and manageable Work Breakdown Structure. Coding and testing of subsystem modules will follow the same hierarchical pattern of development with the highest or top level of system modules being coded and tested first.

Structured Programming. At the basic level, structured programming will deal with the elimination of the "GO TO" statement within individual program modules. The structured program will contain the following basic structures:

1. Sequences of two or more operations.
2. Conditional branches to one of many operations and return (i.e., IF Y THEN A ELSE B).
3. Repetition of an operation while a condition is true.

Emphasis will be placed on restricting individual program modules to have a single entry and a single exit.

Programming Teams. Programming Teams will consist of the lead programmer/analyst, a backup programmer/analyst, and other team members. The lead programmer/analyst will be a senior software engineer responsible for the detailed development of a subsystem. The backup programmer/analyst will assume the duties of the lead programmer/analyst in the event of illness, etc. There will be a central repository of all documentation, listings, source checks, and other paperwork associated with the project.

Structured Walkthroughs. The "Structured Walkthrough" is a generic name given to a series of reviews, each with different objectives and each occurring at different times in the software development cycle. It has six basic characteristics:

1. A walkthrough is arranged and scheduled by the software developer.
2. Management does not attend.
3. Materials are handed out ahead of time.
4. Objectives are clearly communicated to attendees.
5. Emphasis is put on error detection rather than correction.
6. All technical members of the project team have their work product reviewed.

A typical walkthrough will include three to five people with someone designated as recording secretary. This person records all the errors, discrepancies, deficiencies and inconsistencies that are uncovered during the walkthrough. This record becomes an action list for the reviews and a communication vehicle for the reviewers. Walkthroughs are very effective in achieving better quality programs that are less costly to maintain. Walkthroughs are also effective in improving the testing, debugging, and documentation of the programs.

Unit Development Folders. Unit Development Folders is a notebook used for recording everything about a piece of software will be a way of comparing milestones to their schedules and a scheme for verifying that they have been completed. They will provide a uniform and visible collection point for all documentation and code associated with a software module. They will impose a development sequence, establish a timeline, create audit trails, assume useful documentation, reduce turnover problems, and enforce modularity. The folders will be kept available and open to inspection at any time. They will be in a central location independent of the programmers' control.

3.2.6.3.2 Design Tools

The following categories of design tools will be used to develop the BCU software:

- a. Graphic Tools
- b. Design Languages

Graphic Tools. Graphic tools depict processing in a module in a pictorial form. Graphic tools make use of a distinct symbology that enables representation of structured programming constructs. The graphic tools that will be used are:

- a. Functional Diagrams - A diagram representing the functional relationships among the parts of a system.
- b. Structure Charts - Hierarchical charts showing the functional decomposition of a design into subfunctions
- c. Data flow diagrams - Diagrams showing the flow of data between different software functions.

Design Languages. Structured English, also called pseudo code, will be used to provide a means of representing data and processing (the structured constructs) in a textual form. A design language provides a set of well defined structures that allows the writing of a software design in a form that is easy to understand and can be translated into a computer language.

3.2.6.3.3 Programming Standards

Program modules will be kept to a manageable length and will be segmented into reasonable amounts of logic that is easily understood. Attempts will be made to keep modules small and concise, usually between 50 to 100 lines of code. Modules will be self-explanatory due to the inclusion of meaningful comments and a header section defining the input, process and output functions of the module.

3.2.6.3.4 BCU Software Structure

The structure of the BCU software is shown in Figure 3.2.6-11. This section will briefly describe the BCU software in terms of inputs, outputs, and processing functions.

Inputs

- a. Raw data responses from the Scatterometer are received via the HP1000 to BCU micro-processor interface.
- b. The various software activities that perform monitoring and evaluation of Scatterometer instrument operations are invoked via operator entry on CRT menu displays.
- c. Magnetic tapes that were created on the BCU can be retrieved by the BCU for future processing.

Outputs

- a. Menu displays are displayed on the CRT screen to allow the BCU operator to interact with the BCU software.
- b. Real-time data is displayed on the CRT screen during real-time tests.
- c. Test procedure sequences are displayed on the CRT screen during real-time tests.

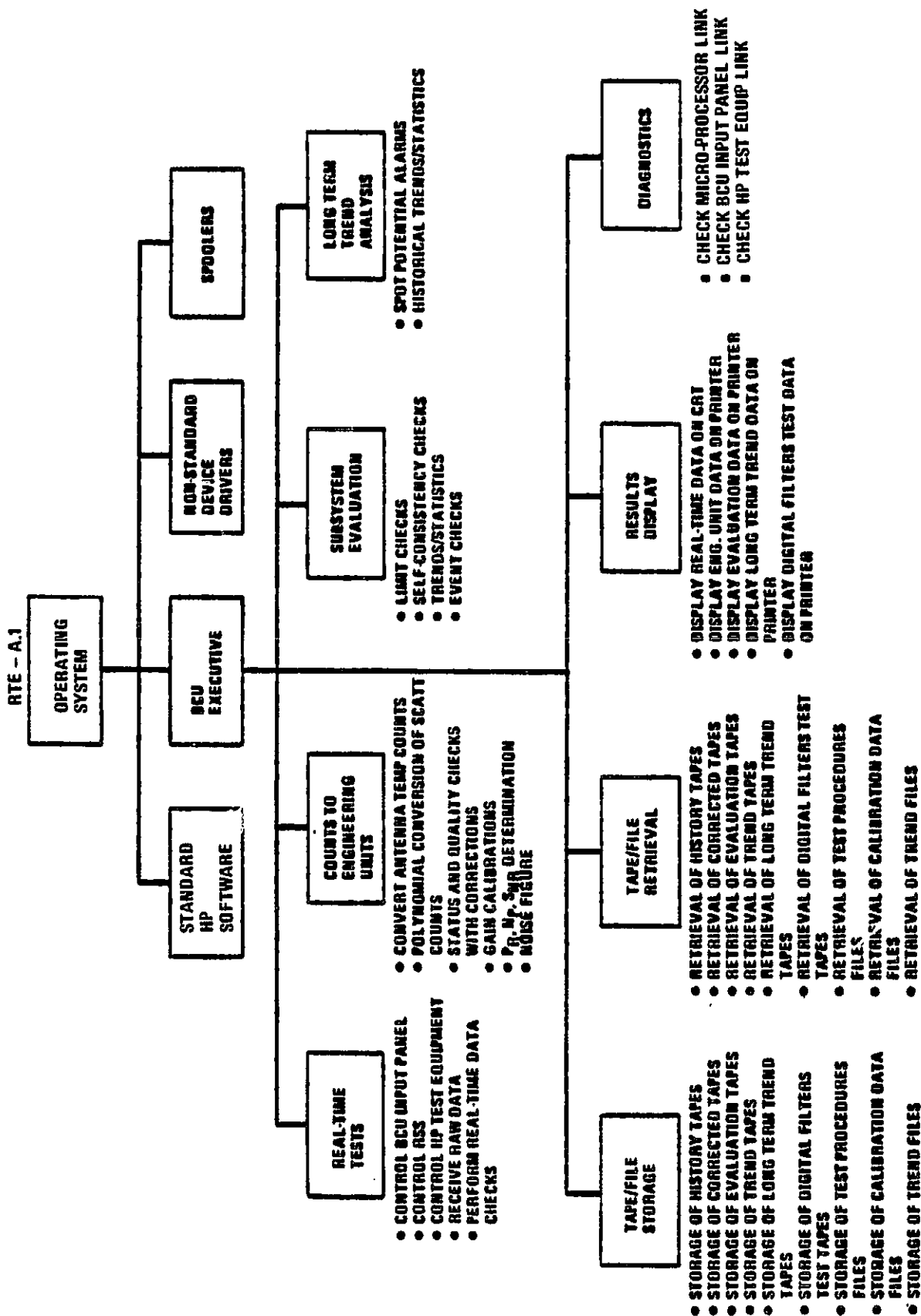


Figure 3.2.6-11. BCU Software Structure

- d. Engineering unit data can be displayed on the line printer in various formats.
- e. Evaluation data can be displayed on the line printer in various formats.
- f. Long-term trend data can be displayed on the line printer in various formats.
- g. Digital Filters test data can be displayed on the line printer.
- h. Responses to operator input are displayed on the CRT screen.
- i. Various types of magnetic tape data can be created.
- j. Various types of disk files are created.

Processing

- a. Automated real-time tests are conducted from command sequences stored in disk scenario files.
- b. Raw response data from the Scatterometer is converted to engineering unit values.
- c. Various checks are performed in the real-time data received.
- d. Subsystem evaluation is performed and parameter statistics of sensor performance are maintained.
- e. Long term trend analysis is performed to spot potential alarm situations. Long term historical trend data is computed for subsystem analysis.
- f. Diagnostics are used to check the status of the various BCU links.
- g. Various reports are formatted for line printer display.
- h. Various CRT displays are formatted for operator observation.

SECTION 4 ✓
RISK AREAS

SECTION 4

RISK AREAS

4.1 HIGH VOLTAGE POWER SUPPLY (HVPS)

The High Voltage Power Supply is one of the risk items for long life missions. This is due primarily to two causes. Corona effects gradually work away at HV potting compounds and insulation so that any flaws in these materials gradually succumb to electric field stresses and breakdown occurs, and any arcing in the high voltage components (including the TWT) and wiring causes stresses on the semiconductors of the power supply such that they could eventually fail.

In an effort to eliminate the first of these causes of failures GE has a long history of improvements in materials and processes aimed at eliminating the microscopic weaknesses in materials which eventually lead to breakdowns. This process of improvements is on-going and, even though the SASS HVPS was the ultimate for MTBF in its day, present technology is permitting even longer life and higher reliability. New circuit designs are also being implemented for protecting circuitry against the effects of arcing and more rugged circuit components are being identified. Life test data is being accumulated on various new techniques. Most of the improvements are being made in conjunction with the BS 2 program where GE is designing and building High Voltage Power Supplies.

Although it is hard to quantify the reliability and life of an HVPS it is felt that the SASS design can meet the NROSS life requirement, but at a higher risk than any of the other components (except TWT). In order to improve the probabilities it would be desirable to incorporate as many of the recent improvements as possible; however, due to the limited resources for this study and the ROM costing exercise the costs do not reflect any of these improvements and are, in fact, for "build to print" SASS designs.

It is suggested that a study contract between now and the start of the NROSS program aimed at defining and costing HVPS product improvements would be desirable for reducing mission risks. Some improvements which could be considered for incorporation are described below:

1. BS-2 Style high voltage transformers, with unpotted primary windings. This prevents crack propagation from primary to secondary, a common failure mode.
2. Arc protection circuits similar to those designed for BS-2 HVPS.
3. Stress Analysis of modules using an advanced finite element techniques to assure low-stress design having lower risk of crack propagation.

4.2 TRAVELLING WAVE TUBE (TWT)

The TWT will be similar to that used for Seasat, with scaling of the internal cavities to operate at the new frequency. Scaling the slow wave coupled cavity structure somewhat to achieve operation at 13.995 GHz should not cause any problems and no increase in cathode current density is expected. The TWT redesign is thus low risk, since the 14.6 GHz TWT used for SASS had already been redesigned from the 13.6 GHz design used for CW operation in BSE. Of greater importance, however, is the limited lifetime expected of about 3 years for operation within specs. Normal degradation of the TWT will result in out-of-specification conditions prior to the end of five years in orbital operations.

4.3 FREQUENCY SOURCES

The 5 MHz reference frequency source is highly reliable and of low risk. It is currently flight qualified and used in DSCS III. This source drives a Solid State Source/Local Oscillator that is identical to the Seasat unit except for minor adjustments in the multiplier circuits to accommodate the change in operating frequency. The SSS/LO is thus of low risk also.

4.4 DIGITAL PROCESSOR

The Digital Processor is a high risk area because it has never been done before for a flight instrument. The GE IR&D project which built a breadboard FFT processor does prove that the "Advance Computational Element" LSI chip, designed by GE, does work in an FFT processor. However considerations of power, speed, reliability and accuracy are issues which will be seriously worked for the first time on the NROSS project.

The risks basically fall into two categories, those associated with new ground being broken by the FFT processor and those resulting from considerable circuitry to be designed in a very limited amount of time. In the first category fall such items as:

1. Establishing band splitter requirements and performance characteristics (Phase error and amplitude imbalance effects, etc.)
2. Aliasing problems
3. Cell-to-cell rejection
4. Dynamic range and resolution (word length requirements)
5. Cumulative processing errors (rounding errors)
6. Band overlap
7. Determine optimum windowing technique
8. Performance verification (complicated by co-registration)

In the second category there are no new or unique problems but merely much circuitry to design in a limited amount of time, new devices to be evaluated for reducing power consumption or size (CMOS memory, faster A/D converter, etc) and some alternative schemes to be evaluated for on board co-registration.

The solution to minimizing these risks is to provide more up-front time to do the required studies for the FFT and to permit an orderly evaluation of alternative designs and advanced devices. It is recommended that a study/development phase be implemented between now and the start of the program to do the following tasks:

1. Determine band splitter requirements and breadboard and test at least one band.
2. Determine word length requirements for A/D Conversion, FFT processing, accumulation.
3. Determine optimum windowing scheme
4. Determine co-registration requirements (such as number of orbit updates) and select an optimum circuit design from several options presently identified.

5. Design and build a breadboard of the digital processor, including: sampling, A/D conversion, buffer memory, FFT processor, Hann weighting (or other windowing) circuits, power estimation, accumulation, and co-registration.
6. Using the above breadboard evaluate candidate advanced devices such as: Sample/Hold circuits, A/D converters, CMOS memory, etc for optimizing speed, power, reliability, and size.
7. Using the breadboard measure and characterize processor performance.
8. Using the breadboard determine and verify a cost effective procedure for testing the processor performance. (With co-registration the number of combinations of doppler center frequencies is large - how can filter performance be best verified at all orbit positions).

Putting many men on a job to meet a schedule milestone usually results in loss of efficiency. By doing some of the suggested up-front work the schedule is effectively doubled and the resulting increased efficiency should result in some reduction of total program cost in addition to minimizing risks.

4.5 DOWNCONVERTERS

The XMIT Downconverter design will be modified from that of the Seasat A Scatterometer to improve system reliability by substitution of a double balanced mixer for the single diode mixer used in the Seasat A Scatterometer upconverter. This will result in a low risk component. The Receive downconverter used in the NROSS Scatter- ometer receiver will be similar or identical in form to the Seasat design, but adjusted principally to accommodate the change in operating frequency. They too will thus be low risk designs.

4.6 RECOMMENDATIONS

Most of the sensor subassemblies are designed to have or can be designed to have an acceptable reliability and/or performance over the three (3) year specified mission life. However, two special cases are considered high risk areas, and, it is recommended that some effort be applied before contract award to minimize this risk. They include the HVPS and the digital processor. The HVPS is selected because of its unusual internal electrical/mechanical stresses and the unpredictable result of these stresses over the mission life; and, the digital processor because the application of the FFT to this purpose advances the state-of-the-art and characterizations of its performance to measure σ^0 (K_p variance) would significantly minimize design risk.

The following activity is recommended for each:

HIGH VOLTAGE POWER SUPPLY

1. perform a stress analyses of the individual potted modules
2. identify high stress areas
3. recommend alternative solutions (if required)
4. fabricate a typical module incorporating selected improved design
5. perform an accelerated test to verify design life.

DIGITAL PROCESSOR

1. develop analytical model to determine performance under selected variables (SNR, number of bits, control stability, etc.)
2. breadboard one 256 point FFT channel capable of processing a signal simulating the expected return signal spectral bandwidth
3. test for performance characteristics (stability, dynamic range, etc.) over the selected input variables (uncertainties)
4. plot data-submit report.

SECTION 5
SUBCONTRACTOR ITEMS

SECTION 5.0 SUBCONTRACTOR ITEMS

The subcontractor data for the NROSS proposal was developed from the data used for the NOSS proposal during the 1980-1981 time frame. The vendors chosen for the NOSS proposal were asked to update their quotes to the 1983 time frame for the NROSS proposal.

All vendors responded with a budgetary or N.T.E. quote based on their 1980 input for NOSS. The following are the vendors that submitted a quote.

- Hughes Edd - Traveling wave tube
- TRW Microwave (formerly Aertech) - L.N.A. and mixer/preamplifier
- Electro Magnetic Sciences - Antenna switching matrix and fixed ferrite devices
- Micro Semiconductor Corp. - KU band solid state noise source
- R.D.L. - Solid state source and local oscillators
- Aerojet - Antenna subsystem

Quotes were for 1 (one) each of an engineering model, a flight unit and a flight spare.

Costs for each unit or for non-recurring and recurring costs were not supplied. The subcontracts are being handled through the Subcontracts sub-section of the Materials organization at General Electric.

SECTION 6
SPARES

SECTION 6
SPARES

It is recommended that one each flight qualified subcontractor item and a complete set of General Electric procured piece parts be supplied as spares. These spares are included in the NTE cost submitted with the Final Report.

The subcontractor spares include the following items:

<u>NAME</u>	<u>QUANTITY</u>
Antenna Switching Matrix (ASM)	1
Ferrite Isolators	1 Each Type
Solid State Local Oscillator Assembly (SS/LO)	1
Travelling Wave Tube (TWT)	1
Low Noise Amplifier (LNA)	1
Frequency Source	1
Antenna	1 Each Polarization

Possibility of a spare HVPS to match the TWT characteristics should be considered during the design phase and will be supplied assuming concurrence by JPL. This decision will be driven by the similarity/dissimilarity of the TWT operating voltages and the expected reliability of the final design product.

SECTION 7
SEASAT A SCATTEROMETER RESIDUAL HARDWARE

SECTION 7

SEASAT A SCATTEROMETER RESIDUAL HARDWARE

Three factors significantly affect the utility of the existing SASS residual hardware. One is the change in frequency of the radiated signal from 14.6 GHz to 13.995 GHz; the second is the allowable space to install the hardware aboard the NOAA-D bus; and, the third is the age of the hardware. Consideration to each principal section of the scatterometer and the possibility of use of each component is given below.

7.1 TRANSMITTER

The transmitter assembly includes the SSLO, the TWT, the ASM, the HVPS, the antenna and various waveguide components such as couplers, ferrites, attenuators and downconverters.

Hughes EDD has been queried regarding modification of the TWT to the new frequency and have replied in the negative stating that to disassemble the TWT and modify the various resonant cavities would be equivalent to fabricating a new EM TWT.

The SSLO is a usable item and will be returned to the vendor for adjustment to the new frequency. This unit can be used for engineering development tasks or as a flight spare. In the latter case, careful analysis must be performed to assure that the assembly does not contain some shelf life limited materials/hardware.

The ASM contains resonant cavities and is specifically designed to operate at the selected frequency. An assessment as to its utility during the NROSS SCATT program was not completed. However, this unit is believed to fall into the same category as the TWT.

The HVPS contains one module (the grid controller) which is not flight qualified. In addition, each power supply is tailored to operate with a particular TWT to accommodate the final anode voltages and currents within a very tight tolerance. Assuming the voltages and currents required by the TWT fall within the range supplied by the HVPS, and the grid module is replaced, there is still the uncertainty of the potting material/assembly shelf life characteristics.

Our present evaluation indicates that this assembly may be usable as an EM and as a backup to the flight unit.

The residual antenna hardware consists of some waveguides, assembly fixtures, shipping containers, and the EM (half section) antennas developed for the previous 14.6 GHz frequency. Aerojet General has evaluated this hardware and can use the waveguides, the assembly fixtures (with some modification) and the shipping containers.

Many waveguide components are unaffected by the frequency change and can be used either as flight or as EM units depending on the space/volume allocated to the T/R assembly and the resultant packaging configuration. Use of each component can be determined when this information becomes known.

7.2 RECEIVER

The receiver consists of a solid state noise source, a low noise amplifier (LNA) downconverters (2) and IF amplifiers.

The LNA used on SASS applied tunnel diodes. The LNA intended for use on NROSS will use GaAs FET amplifiers for their desirable characteristics of higher input saturation and low noise figure. The SASS LNA is not considered a usable component for the NROSS SCATT program.

The solid state noise source may be usable "as is" with satisfactory calibration at the new frequency and assuming there are no shelf life limiting parts within the assembly.

The downconverters and IF amplifiers may be usable, again, assuming that there are no shelf life limiting parts within the assemblies and can be adjusted to the new frequency. These components, however, are "off-the-shelf" type devices and the cost to certify for flight compared to purchasing new hardware may not be justified.

7.3 ANTENNAS

Antenna residual inventory consists of many lengths of waveguide, fabrication fixtures, EM assemblies, a mass model, and shipping containers.

The waveguide lengths are usable.

The fabrication fixtures are designed to enable assembly of a dual polarized antenna. Possibility exists for modifying these fixtures to the single pole antenna required for NROSS with some cost saving.

The EM assemblies (half length) are cut to the SASS 14.6 GHz frequency and are not considered useful.

The mass model can be used with some adjustment to compensate for the difference in NROSS antenna design. The attachment point interface is presently not known and may make use of this item impractical.

Shipping containers are usable with some modification to accommodate the longer (4 inches) antenna.

7.4 INTEGRATED ELECTRONICS ASSEMBLY (IEA)

Residual inventory for this assembly consists of piece parts, PWB, magnetic assemblies and chassis assemblies.

The NROSS IEA is a completely new design. For this reason, only a very limited number of piece parts are considered usable.

SECTION 8
BUDGETARY COST

SECTION 8

BUDGETARY COST

Budgetary (NTE) Costs for design, development, test and integration of one (1) protoflight model is provided under separate cover. This NTE cost includes all manpower and material to deliver one protoflight model, mechanical and electrical ground support equipment, test software, one mass model, two (2) drill fixtures, and spares hardware as listed under Section 6.0.

Cost data was based on the RFP Statement of Work (SOW) and Exhibit 1 of the RFP entitled "Design Requirements for the Scatterometer System for the NROSS Spacecraft" and the following listed appendices.

Appendix A: Work Breakdown Structure

Appendix B: Work Breakdown Structure Task Description

Appendix C: Compliance Matrix Design Requirements for the Scatterometer System for the NROSS Spacecraft.

APPENDIX A
NROSS SCATTEROMETER
WORK BREAKDOWN STRUCTURE (WBS)

<u>WBS ELEMENT</u>	<u>GE WBS CODE</u>
NROSS SCATTEROMETER PROGRAM	00.
<u>PROGRAM MANAGEMENT</u>	10.
Project Office	10.10
Project Office Staff	10.10.01
Contract Administration	10.10.02
Program Travel and Living (distributed)	
Technical Management	10.20
Chief Engineer	10.20.01
Performance Assurance Manager	10.20.02
Manufacturing Manager	10.20.03
Subcontract Management	10.20.04
Resources Management	10.30
Schedule Control	10.30.01
Financial Control (includes CPMS)	10.30.02
Materials	10.30.03
Configuration Management	10.40
Documentation	10.50
Technical Publications	10.50.01
Word Processing	10.50.02
<u>SYSTEM ENGINEERING</u>	11.
System Analysis and Design	11.10
<u>SYSTEM ANALYSIS (includes Math Models)</u>	11.10.01
Link Calculations	11.10.01.01
Error Analyses and Budget	11.10.01.02
Measurement Requirements	11.10.01.03
Command and Data Management (included in 11.30)	
Calibration Requirements	11.10.01.05
Return Signal Simulation	11.10.01.06
Cell Co-Registration	11.10.01.07
Failure Mode Effect Criticality (in 17.10.01)	
Reliability Analyses (in 17.10.01)	
Digital Filter and Proc'r Design	11.10.01.10
Electronics Circuit and Gain Stability	11.10.01.11
In-Orbit Calibration Requirements	11.10.01.12
RFI/EMI and Isolation Requirements	11.10.01.13

<u>SYSTEM DESIGN</u>	11.10.02
Test Plans and Procedures Requirements	11.20
Interface Definition	11.30
System Safety	11.40
<u>INTEGRATION AND TEST PLANS AND PROCEDURES</u>	12.
Electrical Subsystems	12.10
Mechanical Subsystems	12.20
System Integration, Functional and Performance	12.30
Test Plans and Procedures	
Environmental Test Plans and Procedures	12.40
Calibration Procedures	12.50

NOTE: X = 13. IN ALL COMPUTER TABULATED DATA.

<u>SCATTEROMETER INSTRUMENT</u>	X
<u>ANTENNAS</u>	X.10
GE Integration	X.10.01
Antennas Subcontract	X.10.02
<u>TRANSMITTER</u>	X.20
Transmitter Integration	X.20.01
Solid State Source/Local Osc.	X.20.02
Upconverter	X.20.03
Travelling Wave Tube	X.20.04
High Voltage Power Supply	X.20.05
Directional Detector	X.20.06
Antenna Switching Matrix	X.20.07
Waveguide Components	X.20.08
<u>RECEIVER</u>	X.30
Receiver Integration	X.30.01
Calibration Assembly	X.30.02
RFI Filter	X.30.03
Low Noise Amplifier	X.30.04
First Mixer (Down Converter)	X.30.05
Waveguide Components	X.30.06
<u>INTEGRATED ELECTRONICS ASSEMBLY (IEA)</u>	X.40
IEA Integration	X.40.01
Second Mixer and I.F.	X.40.02
Signal Processor	X.40.03
Digital Controller	X.40.04

INTEGRATED ELECTRONICS ASSEMBLY (IEA) (Continued)

DC/DC Converter	X.40.05
IEA Harness	X.40.06
IEA Structure	X.40.07

STRUCTURAL AND THERMAL X.50

Structure (Enclosure)	X.50.01
Thermal Protection	X.50.02
System Harnesses	X.50.03
External Waveguide	X.50.04

INTEGRATION, FUNCTION AND PERFORMANCE TESTS X.60

DELETED X.61

ENVIRONMENTAL TESTS X.70

CALIBRATION X.80

HI-REL PARTS X.90

INSTRUMENT GROUND SUPPORT EQUIPMENT/SOFTWARE 16.

Bench Check Unit (BCU) 16.10

- Cabinet - Three Bay
- AC Power System
- AC Power Cable
- Time Code Generator
- Osc./Pulse Gen. Panel
- Output Interface Panel
- Microprocessor Assembly
- Power Supply
- Power Control Panel
- Modem
- Strip Chart Recorder
- Internal Cables/Harnesses
- BCU Minicomputer
- Test Adapters/Harnesses
- Self-Check Panel
- Recorder Switch Panel
- Oscilloscope
- RSS Interface Panel
- In-Plant BCU Maintenance

RETURN SIGNAL SIMULATOR (RSS) 16.30

<u>HIGH VOLTAGE POWER SUPPLY (HVPS) TEST SET</u>	16.35
<u>Test Software</u>	16.40
Management Plan and Control	16.40.01
Requirements and Preliminary Design	14.40.02
Requirements	16.40.02.01
Preliminary Design	16.40.02.02
<u>Software Design/Code/Debug</u>	16.40.03
Initialization S/W	16.40.03.01
Data Acquisition S/W	16.40.03.02
Data Storage S/W	16.40.03.03
Data Retrieval S/W	16.40.03.04
Data Conversion S/W	16.40.03.05
Data Evaluation S/W	16.40.03.06
Result Output S/W	16.40.03.07
Diagnostic S/W	16.40.03.08
Trend Analysis S/W	16.40.03.09
Utility S/W	16.40.03.10
<u>Documentation</u>	16.40.04
Test Plan	16.40.04.1
Test Procedure	16.40.04.02
User Manual	16.40.04.03
PPS&C	16.40.04.04
<u>Configuration Management</u>	16.40.05
<u>Testing and Maintenance</u>	16.40.06
Software I/F Testing	16.40.06.01
Data Base Maintenance	16.40.06.02
Hardware Integration Tests	16.40.06.03
<u>Machine Time</u>	16.40.07
<u>Shipping and Handling Equipment</u>	16.50
MGSE Integration	16.50.01
Instrumentation Shipping Containers	16.50.02
Lift Sling	16.50.03
Turnover Dolly	16.50.04
Drill Fixtures	16.50.05
Waveguide Shipping Containers	16.50.06
<u>Calibration Equipment (excl. RSS) and Mod's</u>	16.60
<u>Special Test Equipment</u>	16.70
<u>Manufacturing Tooling</u>	16.80

PERFORMANCE ASSURANCE

17.

Reliability	17.10
Reliability Assessment	17.10.01
Failure Reporting and Analysis	17.10.02
Quality Assurance	17.20
MR Coding/Rec. Insp. Planning	17.20.01
Process Control	17.20.02
MRB/Nonconformance Activity	17.20.03
Materials & Processes (Materials Acceptance)	17.20.04
Vendor QA	17.20.05
Receiving Inspection	17.20.06
Parts Engineering	17.20.07
Parts Laboratory	17.20.08
Safety (see WBS 11.40)	17.20.09

FIELD SUPPORT

18.

Integration and Test Support (S/C Level)	18.10
Support of Mission Contractor Meetings	18.10.01
Scatterometer Instr. Integration & Test at Mission Contractor	18.10.02
EM Integration and Test (None)	18.10.02.01
FM Integration and Test (one electronic assy)	18.10.02.03
IGSE Maintenance and Modification	18.10.02.05
Launch Support	18.20
Open	
Post-Launch Evaluation	18.40
Shipping	18.50

SPARES

19.

Procured Spares	19.10
Spares Test, Storage and Administration	19.30
Spares Definition	19.40

APPENDIX B
NROSS SCATTEROMETER
WBS TASK DESCRIPTION

WBS CODE

10.00 PROGRAM MANAGEMENT

The contractor's Project Manager shall have full responsibility and authority to manage and administer all phases of the contract. This encompasses all efforts required to provide program management functions for the prime contract and for all major subcontracts. It includes program planning, technical direction, schedules, budgets, resources control, configuration management, staffing, procurement, reporting, and control of all program efforts. The Project Manager must have a direct line of communication to the top management in the event of conflicts between competing projects for the allocation of resources and personnel.

10.10 PROJECT OFFICE

The contractor shall provide all efforts for program technical direction and management including planning and evaluation. The project office has the responsibility for overall technical performance and resource management of the prime contractor and major subcontractors. It is the focal point of all contact with the government, including the scheduling and coordination of all meetings and reviews.

It specifically includes the efforts of the program manager's staff, and contract administration support. This task also includes all travel and subsistence expenses required for contractor and subcontractor personnel to support the program.

10.20 TECHNICAL MANAGEMENT

The contract shall provide technical management over all aspects of the SCATT program including planning and evaluation, technical direction of program effort, and supervision of subsystem managers. It shall include the management, review, and technical performance evaluation for all other work performed by subcontractors.

WBS CODE

The contractor shall establish and conduct a formal program of planned, scheduled, and documented monthly technical progress reviews. The Project Manager shall determine the participants in these reviews. However, JPL reserves the right to attend and participate in any of the contractor's monthly reviews, or in any other project meeting including those with subcontractors.

10.30 RESOURCES MANAGEMENT

The contractor shall provide administrative support to the technical organization and personnel to maintain contractual, financial, and schedule control of the program.

An effective financial reporting and control system shall be established and maintained throughout the contract period. A continuous cost control procedure shall be implemented.

A detailed program schedule shall be established and maintained. Changes in schedule status shall be included in the weekly rapifax and quarterly technical reports.

10.30.01 SCHEDULE CONTROL

This task includes the effort to develop and maintain a master program schedule, including preparation and maintenance of schedules for each task of the work breakdown structure.

10.30.02 FINANCIAL CONTROL

This task includes the effort to prepare and maintain program budgets; the assessments of progress against them; the financial evaluation of changes on the program; the preparation of management and customer financial reports; and implementation of cost control procedures.

10.30.03 PURCHASING

This task includes the purchasing organization effort to procure the parts, materials and services required for conduct of the program.

WBS CODE

10.40 CONFIGURATION MANAGEMENT

The contractor shall establish and maintain a Configuration Control System in accordance with JPL Spec. (TBD) "Configuration Management Requirements." The system shall be defined in a Configuration Control plan that will be submitted in preliminary form with the proposal and to be submitted in detail three months after contract award. The Configuration Control Plan shall provide for establishment of a Configuration Control Board (CCB) at the contractor's facility which shall evaluate and approve all proposed changes prior to implementation. All Class I changes are subject to approval by the JPL; all Class II changes are to be reviewed by the JPL Project Officer for proper classification.

Class I changes are those which impact or modify the sensor technical performance requirements, technical interfaces, and delivery of principal hardware. Class II changes are all changes not falling into the definition of Class I changes.

10.50 DOCUMENTATION

The contractor shall provide all efforts necessary for the compilation, review, reproduction, and distribution of all documentation identified as deliverable items in accordance with (TBD). This task also includes the preparation and maintenance of other required program documentation. Specifically it includes the creative effort to organize or outline the documents preparatory to their generation such as layout and publication services, editing, and other non-technical documentation efforts. Except as specified, all dimensions in documentation shall use the English units. The contractor shall prepare and submit to JPL, operation and maintenance manuals dedicated to the use of the scatterometer instrument and the IGSE. These shall contain pertinent information regarding the use, operations, calibration, maintenance, and handling of the equipment. The manuals shall include procedures, drawings, and diagrams required for normal use, functional checkout, and minor troubleshooting of the equipment.

The contractor shall maintain a dated equipment test log, including records of all pertinent unit test data and unusual occurrences. These logs shall be available to the JPL Project Officer for review and reproduction at the contrac-

tor's facility. Legible carbon copies, or any other form of reproduction, of all pages of the log books shall be submitted to the Technical Officer on a monthly basis. The original books shall be delivered with the equipment.

11.00 SYSTEMS ENGINEERING

The contractor shall provide the efforts required to define the overall instrument design and the design concepts and performance specifications of the elements that are critical to the specified performance of the instruments, as well as the definition of the test, alignment, and calibration requirements and methods.

11.10 SYSTEM ANALYSIS AND DESIGN

The contractor shall perform a performance requirements analysis, including structural and thermal, to assure that the performance requirements can be met. The impact of the spacecraft attitude, orbit antenna squint angle and other effects shall be included in the error analyses and budget. The system design shall be followed by the selected design analysis and tradeoff studies necessary to evaluate the impact on end-item performance in the event of specification noncompliance at the subsystem and component levels. The contractor shall provide the instrument analytical structural and thermal modes. All system and subsystem design specifications shall be generated under this task in accordance with the overall program schedule. The budgets of weight, center of gravity, power, number of commands and telemetry points shall be established for the instrument system by the time of Preliminary Design Review (PDR) and updated throughout the development program.

11.20 TEST PLANS AND PROCEDURES REQUIREMENTS

The contractor shall define requirements for the development and application of test plans and procedures derived from subsystem and system specifications and designs to insure that the material, parts, item, component, subsystem, or system being tested, developed, fabricated, assembled, or integrated are in compliance with JPL Performance Specification (TBD). Included in this task is the establishment of the subsystem and system functional test procedure requirements, the definition of test equipment requirements, and requirements for performance, subsystem, and system testing. The final overall system level test procedure

should be referred to the SCATT performance specification to demonstrate compliance. This task excludes the efforts to prepare test plan and procedure documents, which are covered in WBS 12.00.

11.30 INTERFACE DEFINITION

It is required that the contractor define the instrument and spacecraft interfaces, and generate timely inputs to step releases to the spacecraft Interface Control Document (ICD). The instrument shall be designed to meet the requirements of the specifications for weight, power, volume, and thermal environment.

11.40 SYSTEM SAFETY

The contractor shall provide a System Safety Plan in support of all development, qualification and flight acceptance test activities. The system Safety Plan shall be in accordance with the requirements of NROSS/SCATT safety requirements and shall address hazardous instrument operation and all ground handling operations starting with manufacturing operations and through instrument delivery in order to:

- o Ascertain potentially dangerous operation,
- o Minimize the risk of hardware damage.

12.00 INTEGRATION AND TEST PLANS AND PROCEDURES PREPARATION

The contractor shall prepare subsystem and system plans for environmental qualification test and sensor calibration. This task shall also include the preparation of combined instrument/BCU operation and maintenance manual. These documents shall be reviewed by the system engineering function and approved by the JPL Project Officer before their implementation.

12.10 ELECTRICAL SUBSYSTEMS

Included are the transmitter, receiver and integrated electronics assembly subsystems as required.

12.20 MECHANICAL SUBSYSTEMS

Included are the antenna, electronics housing, thermal control devices and interconnecting waveguides.

12.30 SYSTEM INTEGRATION

Included in this section are the plans and procedures necessary to successfully integrate the SCATT sensor electronics assembly exclusive of the antenna.

12.40 ENVIRONMENTAL TEST

An environmental plan and the required test procedures will be prepared which collectively will demonstrate compliance to the SCATT specification requirements. The plan and procedures will be submitted to the JPL Project Officer a minimum of 30 days before its planned implementation.

12.50 CALIBRATION PROCEDURES

Calibration plans and procedures shall be prepared to fully characterize the performance of the SCATT instrument under the expected orbital environment.

13.00 PROTOFLIGHT MODEL (PFM)

The PFM is a functional and performance scatterometer instrument system. It will consist of one electronics assembly and six (6) antennas. The PFM will verify the design for the specified performance and environmental requirements. All useable Seasat-A Scatterometer residual subsystems, components, and IGSE will be made available to the development program and supplied to the contract as GFE.

13.10 ANTENNAS

The contractor shall procure the Scatt antennas from an acceptable subcontractor. Complete antennas patterns shall be provided for each antenna. To the extent specified in the procurement specification.

13.20 TRANSMITTER

The contractor shall design, prepare drawings, procure parts and materials, and fabricate, assemble and test the PFM transmitter subsystem.

13.30 RECEIVER

The contractor shall design and prepare drawings, and; fabricate, assemble and test the receiver subsystem for the PFM Model.

13.40 INTEGRATED ELECTRONICS ASSEMBLY (IEA)

The contractor shall design, prepare drawing, procure parts and materials, develop IEA breadboards, and; fabricate, assemble and test the IEA subsystem for the PFM Model.

13.50 THERMAL SUBSYSTEMS

The contractor shall provide all effort to design the thermal subsystem for the SCATT sensor. All fabrication and testing of the thermal system to substantiate the PFM design shall be included under this task.

13.60 INTEGRATION, FUNCTIONAL AND PERFORMANCE TEST

The contractor shall integrate the components and subsystems that make up the PFM instrument and support system for purpose of functional and performance testing to determine that the design will meet the SCATT specifications.

13.70 ENVIRONMENTAL TESTS

A complete set of functional and environmental tests are required on the IEA to verify performance and stability at the specified flight environment.

13.80 CALIBRATION

The contractor shall perform a complete set of calibration tests to verify sensor system performance and to compile the necessary data/tables to enable in-orbit performance correction.

16.00 INSTRUMENT GROUND SUPPORT EQUIPMENT (IGSE)

The IGSE shall include all necessary hardware and software support tasks, including assembly, handling, inspection, testing, calibration, maintenance, check-out, integration with spacecraft, launch operations, shipping, and storage.

16.10 BENCH CHECK UNIT (BCU)

The contractor shall provide one BCU which conforms to the Performance specification paragraph TBD. The BCU shall be a self-contained assembly, or group of assemblies, that allows for functional verification and performance demonstration of the instrument during testing, checkout, and calibration when it is not integrated with the spacecraft. The BCU shall realistically simulate all

points of electrical interface with the NOSS spacecraft and will include control of experiment power, command timing functions, and data handling. The BCU shall be capable of real-time recording, and near-real-time data reduction, and conversion of received power into engineering units. It will display instrument performance and state during all phases of test.

16.30 RETURN SIGNAL SIMULATOR (RSS)

The contractor shall provide one RSS unit per the SCATT Performance Specification paragraph (TBD).

16.40 TEST SOFTWARE

The contractor shall generate all necessary deliverable test and calibration and data reduction software to comply with requirements stated under WBS 16.10. The instrument contractor shall prepare limited Software Users and Programmers Manuals as may be required in support of the SCATT instrument integration and test prior to delivery.

16.50 SHIPPING AND HANDLING EQUIPMENT AND PROCEDURES

The contractor shall prepare a plan for packing, transportation, and receipt of the deliverable hardware. The PFM shall be shipped to the NROSS system contractor (TBD). Advance notice of the PFM shipment shall be made by TWX at least 1 week prior to shipment.

16.60 CALIBRATION EQUIPMENT AND MOD'S

The contractor is responsible for design modification (if any) of the BCU during spacecraft integration and check of instrument calibration at the launch site.

16.70 SPECIAL TEST EQUIPMENT

The contractor shall provide any Special Test Equipment (STE) required to test the instrument and its subsystem. STE is defined as any required test equipment which is necessary during the assembly/integration phase and is not available either as an identified IGSE item or from existing test equipment pools.

16.80 MANUFACTURING TOOLING AND TEST FIXTURES

The contractor shall provide tooling and test fixtures as required to perform the contract. This task excludes the drill fixtures, which are identified as IGSE.

17.00 PERFORMANCE ASSURANCE

The contractor shall provide the efforts required for Reliability, Quality Assurance, and Safety based on the provisions delineated in the instrument specifications.

17.10 RELIABILITY

The contractor shall perform reliability analyses at the component level to identify design deficiencies early in the development phase. The reliability engineer will review subcontractor purchased items and recommend action as necessary to improve hardware performance.

17.20 QUALITY ASSURANCE

The contractor shall provide all effort, equipment, and materials necessary to insure adequate quality control for each system, subsystem, component and part from the receiving of material, through manufacturing, inspection, test, and shipping.

This includes the necessary quality assurance documentation to fulfill contractual requirements. This effort will include participation in initial program planning, schedules, customer specification review, vendor survey and design reviews. It will also include providing quality inputs for procurement documents, test and inspection procedures, and implementing corrective action when quality is marginal or unsatisfactory.

17.30 SAFETY

The contractor shall support all efforts necessary in carrying out an approved safety plan and shall implement safety procedures and equipment as appropriate at the manufacturing/test stations.

18.00 FIELD SUPPORT

The contractor shall provide all necessary support from the time the deliverable hardware models leave the contractor's plant through spacecraft integration and environmental testing and prior to launch and during post-launch performance evaluation. Potential modifications due to failures or system interface incompatibilities are not to be included as part of this cost since they cannot be scoped or defined at this time.

18.10 INTEGRATION AND TEST

The contractor shall provide the necessary personnel, services, and equipment to support the SCATT instrument integration with the NROSS Spacecraft. This effort is reserved to an "as required" consulting basis during the antenna array assembly on the spacecraft; during the electronic subsystems assembly and checkout; during calibration checks; and during data analysis. This task will be performed at the spacecraft contractor's facility.

18.20 LAUNCH SUPPORT - SPACE TRANSPORT SYSTEM (STS) INTEGRATION AND TEST

The contractor shall furnish the necessary personnel, services, and equipment to support spacecraft integration and test at the launch facility.

18.40 POST-LAUNCH EVALUATION

The contractor shall support the post-launch instrument checkout, in-orbit performance evaluation, and instrument validation for a period not to exceed thirty (30) days after launch. This effort is limited to data evaluation at either JPL or at a ground control facility.

18.50 SHIPPING AND HANDLING SERVICES

The contractor shall provide services for shipping and handling of the instruments and required support equipment. Items destined for the NROSS System Contractor will be shipped FOB his facility. For cost purposes, an East Coast NROSS Spacecraft Integration Contractor is assumed.

19.00 SPARES

The contractor shall analyze instrument spares requirements and present a recommended list of spares. All spare articles shall be identical and of the same quality as the PFM instrument and shall be certified as flight ready.

19.10 SPARES PROCUREMENT

This includes procurement of all major components, parts, and materials necessary to assure an adequate level of operational spares. As presently conceived these spares will consist of one (each) of the major subcontractor items and the necessary piece parts to repair the flight hardware. A list is included in the Study Final Report. No spares are currently planned for fabrication other than subcontract items.

19.30 SPARES TEST, STORAGE AND ADMINISTRATION

All spares shall be stored in a controlled area certified by the Quality Assurance organization. An inventory by name, serial number, part number, and quantity shall be furnished to the JPL Project Officer prior to delivery of the PFM.

APPENDIX C
COMPLIANCE MATRIX - DESIGN REQUIREMENTS
FOR THE SCATTEROMETER SYSTEM FOR THE NROSS SPACECRAFT

NROSS REQUIREMENTS

<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>	<u>REQUIREMENT</u>	<u>G.E. COMPLIANCE</u>
1.2	INSTRUMENT IDENTIFICATION	THREE ELECTRONIC UNITS & 6 ANTENNAS	TWO ELECTRONIC UNITS & 6 ANTENNAS
1.3	OVERALL TASK DEFINITION	MEET SPECIFIED PERFORMANCE FOR 3 YEARS	G.E. ACCEPTS
2.0	APPLICABLE DOCUMENTS	2.1.X NOSS SPECS TBD'S 2.2.X NASA SPECS 2.3.X DOD PUBLICATIONS 2.4.X JPL PUBLICATIONS 2.5.X NASA CONTRACT REPORTS	G.E. NEEDS G.E. ACCEPTS G.E. ACCEPTS G.E. ACCEPTS G.E. HAS
3.0	REQUIREMENTS	1 1/2 YEARS ON ORBIT PLUS 1 1/2 YEARS DEGRADED PERFORMANCE	G.E. ACCEPTS
3.1	SYSTEM PERFORMANCE	MEASURE OCEAN SURFACE - WIND SPEEDS 4M/SEC TO 24M/SEC + 2M/SEC OR 10% WHICHEVER IS GREATER - WIND DIRECTION 0° - 360° NO MORE THAN TWO ALIASES 180° OUT OF PHASE (90%)	G.E. ACCEPTS
3.1.1	INSTRUMENT DESCRIPTION AND PRINCIPAL OF OPERATION	MEASURE OCEAN NORMALIZED RADAR SCATTERING CROSS-SECTION, σ_0 , AS FUNCTION OF INCIDENCE ANGLE MAKE THREE SEQUENTIAL INDEPENDENT MEASUREMENTS OF σ_0 FOR EACH RESOLUTION CELL	G.E. ACCEPTS G.E. ACCEPTS

GROSS REQUIREMENTS

<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>	<u>REQUIREMENT</u>	<u>G.E. COMPLIANCE</u>
3.1.1	INSTRUMENT DESCRIPTION AND PRINCIPAL OF OPERATION (CONTINUED)	THREE TIME-SEPARATED MEASUREMENTS ON EACH SIDE ARE TELEMETERED TO GROUND FOR PROCESSING	G.E. ACCEPTS
3.1.1.1	MEASUREMENT SWATH	CO-REGISTRATION IS REQUIRED	G.E. ACCEPTS
		BOTH SIDES OF SATELLITE SUBTRACK	G.E. ACCEPTS
		0° TO 60° ON EACH SIDE	G.E. ACCEPTS
		ORBIT ALTITUDE - 830 KM	G.E. ACCEPTS
		NEAR NADIR TRACK IS + 20°	G.E. ACCEPTS
		WIND VECTOR SWATH 20°-60°	G.E. ACCEPTS
		CO-REGISTRATION ONLY REQUIRED IN WIND VECTOR SWATHS	G.E. ACCEPTS
		ANTENNA 1, 2, 3 ARE ON RIGHT SIDE	G.E. ACCEPTS
		ANTENNA 4, 5, 6 ARE ON LEFT SIDE	G.E. ACCEPTS
		ANTENNA 1, 3, 4, & 6 ARE VERT. POL.	G.E. ACCEPTS
		ANTENNA 2, AND 5 ARE HORIZ. POL.	G.E. ACCEPTS
3.1.1.2	MEASUREMENT RESOLUTION	REF. FIG. 3-2 FROM 10KM X 35 KM TO 15 KM X 39KM	G.E. ACCEPTS
		INSTANTANEOUS CELL BASE LENGTH L=35 NOMINALLY FOR ALL ANTENNAS	G.E. ACCEPTS

<u>NROSS REQUIREMENTS</u>															
<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>	<u>REQUIREMENT</u>	<u>G.E. COMPLIANCE</u>												
3.1.1.3	MEASUREMENT GRID SPACING	25KM NOMINAL AT CROSS TRACK DISTANCES OF 187.5KM TO 765.5KM	G.E. ACCEPTS												
3.1.1.4	MEASUREMENT SEQUENCES	24 DOPP. CELL MEAS. USING V POL. ON BOTH XMIT AND REC. ON ANT. 1, 3, 4 & 6 FOLLOWED BY 24 DOPP. CELL MEAS. WITH H POL. ON BOTH XMIT & REC. ON ANT. 2 & 5	G.E. ACCEPTS												
3.1.1.5	MEASUREMENT CO-REGISTRATION ACCURACY	NROSS REQ. IS 12.5KM 1 SIGMA SCATT INSTRUMENT IS ALLOWED 10KM (1 SIGMA)	G.E. ACCEPTS												
3.1.2	RADAR CROSS-SECTION (σ°) MEASUREMENT REQUIREMENTS	TBD	G.E. NEEDS REQUIREMENT												
3.1.2.1	DYNAMIC RANGE	MOST HANDLE ALL RETURN SIGNALS FOR SPECIFIED WIND FIELD CONDITIONS IN WIND VECTOR AND NEAR NADIR SWATHS	G.E. ACCEPTS												
3.1.2.2	RADAR CROSS SECTION (σ°) MEASUREMENT PRECISIONS (RANDOM ERRORS)	SEE TABLES 3-1 THRU 3-6 (TBD)	G.E. NEEDS REQUIREMENT												
3.1.2.3	RADAR CROSS SECTION (σ°) MEASUREMENT PRECISIONS (BIAS ERRORS)	RSS OF ALL BIAS ERRORS < 2.0dB	G.E. ACCEPTS												
3.1.3	ANTENNA REQUIREMENTS														
3.1.3.1	ANTENNA ORIENTATION	<table><tr><th>BEAM NO.</th><th>AZ</th><th>EL</th></tr><tr><td>186</td><td>+45°</td><td>40°</td></tr><tr><td>283</td><td>+65°</td><td>37°</td></tr><tr><td>384</td><td>+135°</td><td>40°</td></tr></table>	BEAM NO.	AZ	EL	186	+45°	40°	283	+65°	37°	384	+135°	40°	G.E. ACCEPTS
BEAM NO.	AZ	EL													
186	+45°	40°													
283	+65°	37°													
384	+135°	40°													

NROSS REQUIREMENTS

PARA. NO.	PARAGRAPH TITLE	REQUIREMENT	G.E. COMPLIANCE
3.1.3.2	ANTENNA POLARIZATION	EACH ANTENNA SINGLY POLARIZED, VERTICAL OR HORIZONTAL 99% PURITY	G.E. ACCEPTS
3.1.3.3	ANTENNA GAIN	SEE TABLE 3-4 GAIN (dB) 16.5 TO 32.5 FOR BEAM ANGLES + 40° TO 0°	G.E. ACCEPTS
3.1.4	TRANSMITTER PERFORMANCE REQUIREMENTS		
3.1.4.1	FREQUENCY	$f_o = 13.995 \text{ GHz}$	G.E. ACCEPTS
3.1.4.2	PULSE WIDTH	$5.0 \times 10^{-3} \text{ SEC}$	G.E. ACCEPTS
3.1.4.3	P.R.F.	52.85 PULSES/SEC	G.E. ACCEPTS
3.1.4.4	DUTY CYCLE	29.15%	G.E. ACCEPTS
3.1.4.5	RF OUTPUT POWER	100W TO 135W	G.E. ACCEPTS
3.1.4.6	PUTPUT POWER VARIATIONS	+ 0.5dB FIRST 15 MIN. + 0.25dB AFTER 12 HRS. LESS THAN -1dB DOWN AFTER 3 YEARS (90W)	G.E. ACCEPTS
3.1.4.7	OUTPUT NOISE POWER DENSITY	< -197.79dB/H _Z IN ANY 100KH _Z BAND	G.E. ACCEPTS
3.1.4.8	SPURIOUS HARMONIC OUTPUT	ALL NON HARMONIC COMPONENTS 50dB BELOW FUNDAMENTAL TOTAL HARMONIC CONTENT MORE THAN 20dB BELOW FUNDAMENTAL	G.E. ACCEPTS

<u>NROSS REQUIREMENTS</u>		
<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>	<u>REQUIREMENT</u>
		<u>G.E. COMPLIANCE</u>
3.1.4.9	STABILITY	SCATT TRANSMITTER MUST BE UNCONDITIONAL STABLE FROM 0 DRIVE TO 3dB ABOVE MAXIMUM
		G.E. ACCEPTS
3.1.4.10	TURN ON TIME	5 MINUTE WARM UP
		G.E. ACCEPTS
3.1.4.11	LIFETIME	3 YEARS IN ORBIT AFTER 300 HRS. (MIN.) IN GROUND TEST
		G.E. ACCEPTS
3.1.5	RECEIVER PERFORMANCE REQUIREMENTS	
3.1.5.1	DYNAMIC RANGE	TBD dB MINIMUM REF - 200dBW RETURN SIGNAL (WIND SPEEDS 4M/SEC TO 24M/SEC + 4dB MARGIN)
		G.E. NEEDS REQUIREMENT
3.1.5.2	DOPPLER FREQUENCY CELLS	$f_D = 420 \text{ KH}_Z$ IN ANY ONE MEASURE- MENT. -2 CELLS NEAR MADIR. -24 CONTIGUOUS CELLS IN WIND VECTOR PATH
3.1.5.3	DOPPLER CORRECTION FOR CO-REGISTRATION	CO-REGISTER ° DATA FROM RESOLUTION CELLS IN BEAM 1, 2, 3 AND 4, 5, 6
3.1.5.4	RECEIVER PROCESSING FIGURE OF MERIT (k_D) OR ($\Delta P_R/P_R$)	TABLES 3-1 TO 3-6 TBD
		G.E. NEEDS REQUIREMENT

PARA.
NO.PARAGRAPH TITLEREQUIREMENTG.E. COMPLIANCE

3.1.7

COMMAND AND OPERATING MODES

NORMAL MODE - SIMULTANEOUS
TRANSMISSION AND RECEPTION -
FULL RESOLUTION AND SWATH
COVERAGE ON BOTH SIDES OF
SUB-SATELLITE TRACK

G.E. ACCEPTS
SINGLE POL. ONLY

<u>MODE</u>	<u>ON</u>	<u>ANTENNAS</u>	<u>POL.</u>
1	T&R	1-6	V, H
2	T&R	1-3	V, H
3	T&R	4-6	V, H
4	STBY		
5	CONT.CAC		

<u>SEQUENCE</u>	<u>DESCRIPTION</u>
SCATT ENABLE	DC/DC CONV. ON
HVPS ENABLE	POWER HVPS
HVPS OFF	REMOVE HVPS POWER
SCATT OFF	DC/DC CONV. OFF

<u>NROSS REQUIREMENTS</u>		<u>REQUIREMENT</u>	<u>G.E. COMPLIANCE</u>
<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>		
3.2.1	SCATT SYSTEM DEFINITION	SAME AS SEASAT A SCATT EXCEPT FOR 1. ADD 2H POL. ANT. (2&5) 2. CHANGE ANT. 1,3,4, & 6 to V POL. 3. CHANGE TO DIGITAL DOPP. FILTERS 4. ADD SEQUENTIAL CHANGES OF DOPPLER CENTER FREQUENCIES (CO-REGISTRATION) 5. CHANGE TO IMPROVE LNA 6. CHANGE TO $f_c = 13.995$ GHz	GE ACCEPTS
3.2.1.1	NROSS SPACECRAFT ORBIT	ALTITUDE -- 830KM \pm 18 KM INCLINATION -- 98.739° ECCENTRICITY -- TBD	OK OK NEEDS REQUIREMENT
3.2.1.3	INTERFACE REQUIREMENTS	TBD	GE NEEDS REQUIREMENT
3.2.1.3.1	ELECTRICAL		
3.2.1.3.1.1	POWER	1. INPUT VOLTAGE 28 ± 0.6 VDC 2. POWER CONSUMPTION $250W_{MAX}$ 3. REG. RIPPLE o 5-100KHz <100MV P-P o SPIKES <100MV & 11MS < 50,000 PPS 4. UN REG RIPPLE o 30 Hz - 1MHz < 500 MV P-P o SPIKES <4VP <10 MS 5. CURRENT TRANSIENTS $\leq 10^5$ AMPS/SEC	GE ACCEPTS
3.2.1.3.3.2	COMMANDS	DISCRETE RELAY FUNCTIONS TBD IMPULSE LOGIC SWITCHES TBD	GE NEEDS REQUIREMENT

NROSS REQUIREMENTS

<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>	<u>REQUIREMENT</u>	<u>G.E. COMPLIANCE</u>
3.2.1.3.3	RF CLOCK INPUT & TIMING	SCATT GENERATES REQUIRED FREQUENCIES	GE ACCEPTS
3.2.1.3.4	DATA	DATA RATE FROM SCATT = 3.0 Kbps FORMAT TBD	GE NEEDS REQUIREMENTS
3.2.1.3.5	TELEMETRY	TBD	GE NEEDS REQUIREMENTS
3.2.1.3.6	SWITCHED TELEMETRY BUS	TBD	GE NEEDS REQUIREMENTS
3.2.1.3.7	MECHANICAL CHARACTERISTICS	VOLUME TBD WEIGHT TBD	GE WILL STATE ITS DESIGN
3.2.1.3.8	THERMAL REQUIREMENTS	SCATT WILL PROVIDE ITS OWN THERMAL CONTROL TO MAINTAIN OPERATING 1. TEMPERATURES OP 0°C TO +35°C NON-OP -10°C TO +55°C 2. POWER DISSIPATION PER PARA. 3.2.1.3.1.1	GE PROPOSES THERMAL LOWER
3.2.1.4	INTERFACE DEFINITION & CONTROL	GE RESPONSIBLE FOR ICD	GE ACCEPTS
3.2.1.5	OPERATING CONDITIONS	3 YEARS IN ORBIT	GE ACCEPTS
3.2.1.5.1	PRE-LAUNCH ENVIRONMENTS	FAB, INTEG. QUAL, ACCEPT.	GE ACCEPTS
3.2.1.5.2	RANDOM VIBRATION	HANDLING, STORAGE, TRANSPORTATION LAUNCH SITE Hz g2/Hz 10 - 20 .01 20 - 80 +10dB/OCT. 80 - 600 .04 600- 2000 -10dB/OCT. COMPOSITE 7.0 g rms	GE ACCEPTS

<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>	<u>REQUIREMENT</u>	<u>G.E. COMPLIANCE</u>
<u>NROSS REQUIREMENTS</u>			
3.2.1.5.2 (CONT.)	QUASI-STATIC LOADS (g's)	X ±6.5 Y ±3.0 Z ±5.0	GE ACCEPTS
	FACTORS OF SAFETY	YIELD 1.4 ULTIMATE 1.8	GE ACCEPTS
3.2.1.5.2.3	PRESSURE	FIGURE 3.3 TBD	GE NEEDS REQUIREMENT
3.2.1.5.3	ORBITAL ENVIRONMENTS		
3.2.1.5.3.1	EMI/RFI	o CHAPTER 3 PA REQUIREMENT TBD o MUST MEET NROSS S/C ENVIRONMENT	GE NEEDS REQUIREMENT
3.2.1.5.3.2	RADIATION	TBD	GE NEEDS REQUIREMENT
3.2.2	SYSTEM ENGINEERING	- INST. PERFORMANCE - PROD. ASSUR. REQUIREMENTS - CONCEPTUAL DESIGN - SUBSYSTEM DESIGN ANALYSIS - INTEG., PERF., QUAL. ACCEP. - CALIBRATION T.P.'S	
3.2.2.1	STUDIES & ANALYSES	1. ERROR ANALYSIS & BUDGET 2. MEASUREMENT REQUIREMENTS 3. COMMAND & DATA MANAGEMENT 4. STRUCTURAL & THERMAL 5. CALIBRATION 6. RETURN SIGNAL SIMULATION 7. CELL REGISTRATION 8. DIAGNOSTIC SELF CHECKING 9. FAILURE MODES 10. DIGITAL FILTER & PROC. 11. ELECTRONIC CIRCUITS	GE ACCEPTS
3.2.2.2	MATERIAL	DEVELOP MAT & PROC.	

NROSS REQUIREMENTS

<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>	<u>REQUIREMENT</u>	<u>G.E. COMPLIANCE</u>
3.2.3	SUBSYSTEM & SYSTEMS DESIGN	NO PERIODIC MAINTENANCE	GE ACCEPTS
3.2.3.1	DESIGN CONSTRAINTS	MEET JPL DOCUMENT DM 509306	GE ACCEPTS
3.2.3.2	POWER ON RESET	PROVIDE POWER ON RESET	GE ACCEPTS
3.2.3.3	CONNECTOR & GROUND REQUIREMENTS	TBD NROSS REQUIREMENTS	GE NEEDS REQUIREMENTS
3.2.3.4	DIRECT ACCESS	DIRECT ACCESS LINES FOR FAULT ISOLATION	GE ACCEPTS
3.2.3.5	DRILL FIXTURE	TWO MATCHED SETS OF DRILL FIXTURES	GE ACCEPTS
3.2.4	FABRICATION	COMPLY WITH DM 509306	EM UNIT HAS BEEN DELETED
3.2.5	INTEGRATION AND TEST		
3.2.5.1	INTEGRATION AND TEST PLAN	CONTRACTOR MUST SUPPLY TEST PLAN	GE ACCEPTS
3.2.5.2	TEST PROCEDURE	CONTRACTOR SHALL SUPPLY TEST PROCEDURE	GE ACCEPTS
3.2.5.3	ENVIRONMENTAL TESTING	INSTRUMENT SHALL SURVIVE VARIOUS ENVIRONMENTAL TESTS	GE ACCEPTS
3.2.5.4	CALIBRATION TESTS	GENERATE A CURVE OUTPUT VOLTAGE VERSUS RETURNED POWER, PR, FOR EACH DOPPLER CHANNEL USING THE SE	GE ACCEPTS

NROSS REQUIREMENTS

<u>PARA. NO.</u>	<u>PARAGRAPH TITLE</u>	<u>REQUIREMENT</u>	<u>G.E. COMPLIANCE</u>
3.3	INSTRUMENT GROUND SUPPORT EQUIPMENT		
3.3.1	SUPPORT EQUIPMENT (SE) AND CALIBRATION EQUIPMENT (CE)		
3.3.1.1	SUPPORT EQUIPMENT	PROVIDE A MEANS FOR ON-SITE FUNCTION, PERFORMANCE, AND CALIBRATION TESTING AND ACCEPTANCE TESTING OF THE SCATT INSTRUMENT	GE ACCEPTS
3.3.1.2	MISSING		
3.3.1.3	MISSING		
3.3.1.4	AUXILIARY SUPPORT EQUIPMENT	GENERATE LIST OF EQUIPMENT NEEDED	GE ACCEPTS
3.3.2	SHIPPING AND HANDLING	- IN ACCORDANCE WITH TBD NROSS SPACECRAFT/INSTRUMENT INTERFACE REQUIREMENTS - SUPPLY SPECIFICATIONS - SUPPLY INSTALLATION FIXTURE	GE NEEDS REQUIREMENTS GE ACCEPTS GE ACCEPTS
3.3.2.1	SHIPPING CONTAINER	- PACK IN A REUSABLE SHIPPING CONTAINER PRESSURIZED WITH DRY NITROGEN - USE THREE AXIS SHOCK INDICATORS	GE ACCEPTS GE ACCEPTS